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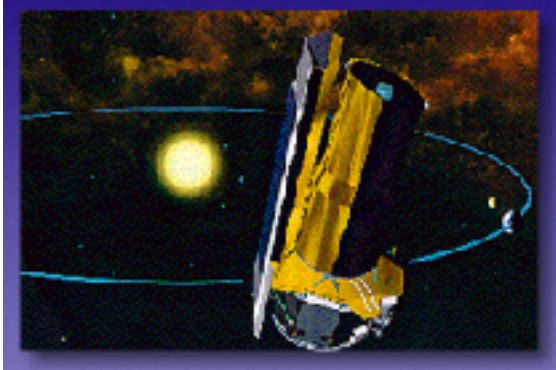
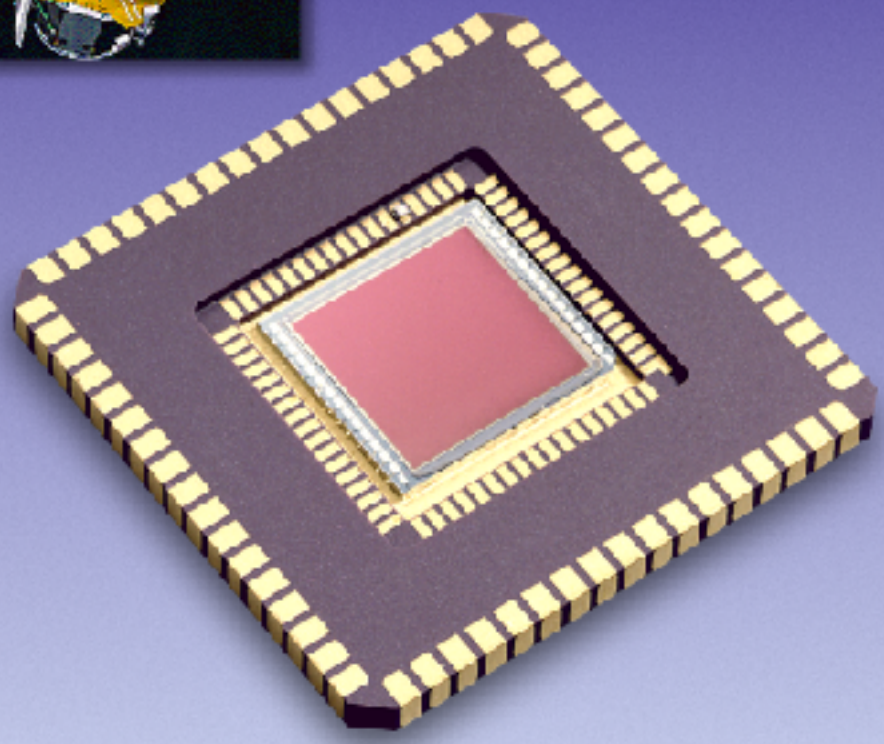
Infrared Operations

CRC-744 256 x 256
The "SIRTF" Readout Integrated Circuit



User's Guide and Operating Manual



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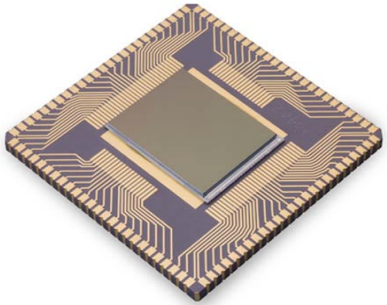
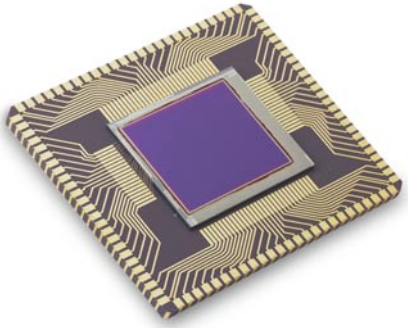
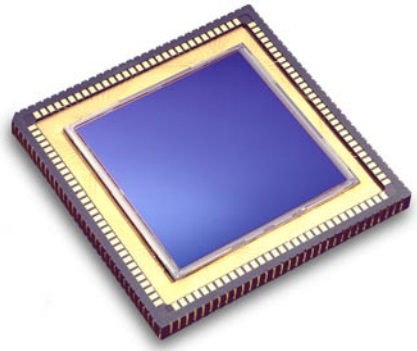
Astronomical Infrared Sensor Chip Assemblies
Standard Products

Raytheon
Infrared Operations

High performance InSb and Impurity Band Conduction (IBC) focal plane arrays are available with spectral responses from 0.4μm to 28μm for ground-based astronomy and space-based instruments. Raytheon Infrared Operations (RIO) is one of the world's leading suppliers of focal plane arrays for astronomical applications for the past 10 years. RIO utilizes state-of-the-art facilities and processes to produce these arrays. Listed below are some of the InSb and IBC arrays available from Raytheon as standard products for astronomical applications. Custom arrays incorporating our latest multiplexer designs are also available in a variety of formats. Raytheon has also developed a double layer heterostructure HgCdTe process for large format arrays. Custom arrays utilizing this process are available for those customers desiring HgCdTe with its ability to tailor the bandgap for any cutoff wavelength.

			
	InSb-IRIS	ALADDIN III Quadrant	ALADDIN III
Format:	512 x 412 (210,944 elements)	512 x 512 (262,144 elements)	1024 x 1024 (1,048,576 elements)
Pixel Size:	30 μm	27 μm	27 μm
Active Fill Factor:	> 98%	> 98%	> 98%
Spectral Response:	0.4–5.3 μm (~flat from 1-5 μm)	0.4–5.3 μm (~flat from 1-5 μm)	0.4–5.3 μm (~flat from 1-5 μm)
Average Quantum Efficiency:	> 80% peak InSb	> 70% (1–5.0 μm)	> 70% (1–5.0 μm)
Typical Response Uniformity:	≤ 5% (1σ)	≤ 8% (1σ)	≤ 8% (1σ)
Average Dark Current:	≤ 1 e^-/sec	≤ 1 e^-/sec	≤ 1 e^-/sec
Typical Integration Capacity:	2.0 x 10^5 e^- (0.06 pF and 0.6V)	2.0 x 10^5 e^- (0.06 pF and 0.6V)	2.0 x 10^5 e^- (0.06 pF and 0.6V)
Mean Input Referred Noise:	10–50 e^- (sampling technique dependent)	8–50 e^- (sampling technique dependent)	8–50 e^- (sampling technique dependent)
Optimal Operating Temperature:	15–30Kelvin	30–35 Kelvin	30–35 Kelvin
Readout Type:	Source Follower per Detector (SFD)	SFD	SFD
Operational Modes:	Destructive or non-destructive readout	Destructive or non-destructive readout	Destructive or non-destructive readout
Compatible Sampling Techniques:	Standard correlated sampling & multiple correlated sampling (Fowler and "up-the-ramp")	Standard correlated sampling & multiple correlated sampling (Fowler and "up-the-ramp")	Standard correlated sampling & multiple correlated sampling (Fowler and "up-the-ramp")
Typical Frame Rates:	1-10 Hz	1-20 Hz	1-20Hz
Number of Outputs:	4 + 2 diagnostic	8	32 (8 per quadrant)
	InSb		
	Low Background		

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Astronomical Infrared Sensor Chip Assemblies
Standard Products

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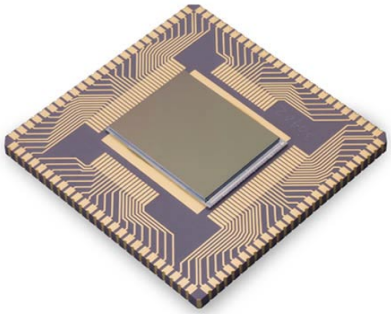
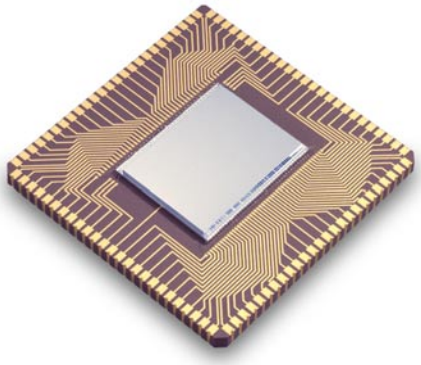
(Science Grade Operability > 99%)		
	IBC-IRIS	
Format:	512 x 412	320 x 240 (76,800 elements)
Pixel Size:	30 µm	50 µm
Active Fill Factor:	≥ 98%	≥ 98%
Spectral Response:	1–28 µm	1–28 µm
Average Responsive Quantum Efficiency:	≥ 40%	≥ 40%
Typical Response Uniformity:	≤ 8% (σ/mean)	≤ 8% (σ/mean)
Average Dark Current:	< 1 e^-/sec (@ T=6K)	< 100 e^-/sec (@ T=6K)
Typical Integration Capacity:	> 1.0 x 10^5 e^- (30 fF and 0.6V bias)	1.0–3.0 x 10^7 e^- (Gain dependent)
Mean Input Referred Noise:	10–50 e^- rms (Sampling technique dependent)	< 1000 e^- rms (CDS, high gain)
Operating Temperature:	4–10 Kelvin	4–10 Kelvin
Readout Type:	Source Follower per Detector (SFD)	Direct Injection (DI)
Operational Modes:	Destructive or non-destructive readout	Integrate-while-read, Integrate-then-read
Compatible Sampling Techniques:	Standard correlated sampling & multiple correlated sampling (Fowler and "up-the-ramp")	Built-in correlated double sampling; multiple sampling can be implemented
Typical Frame Rates:	1-10 Hz	100-500 Hz
Number of Outputs:	4 + 2 diagnostic	16 or 32
	IBC	
	Low Background	**High Background**

256 x 256 and other custom formats in InSb, IBC, and HgCdTe available upon request.

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Raytheon

Infrared Operations

USER'S GUIDE AND OPERATING MANUAL
FOR THE
CRC-744 256 × 256 "SIRTF" READOUT INTEGRATED CIRCUIT

NOVEMBER 1999
(REVISED APRIL 2001)

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Publication No.: MAN01-0325

CONTENTS

ILLUSTRATIONS

Figures **Page**

TABLES

Tables **Page**

CHAPTER 1

1.0 INTRODUCTION TO THE CRC-744

1.1 Background

This manual serves as both a user's guide and operating manual for the CRC-744 readout integrated circuit (ROIC). The "sensor chip assembly" (SCA) is a hybrid structure consisting of a CRC-744 silicon "cryo-CMOS" ROIC interconnected to an infrared photodetector array. The ROIC and detectors are interconnected by an array of indium bumps which provide the electrical interface of the individual detector elements ("pixels") to the corresponding ROIC input unit cells.

The 256 x 256 SCA is designed for cold operation (≤ 5–35 K) at relatively low backgrounds ($\leq 2\times10^{11}$ ph/sec/cm^2) for ground-based and space-based astronomy applications using near infrared InSb (~1 to 5 μm) or longer wavelength infrared Si:As (~2 to 28 μm). These SCAs operate with high quantum efficiency, very low dark currents, excellent uniformity, and low noise.

1.2 CRC-744 Readout Description

The CRC-774 ROIC consists of 256 columns x 256 rows of unit cells each 30 μm by 30 μm in size. The heart of the unit cell is the source follower per detector (SFD) input circuit. An additional source follower buffers the output signal and is capable of driving up to 600 pF of cable, although ≤ 300 pF is recommended. The unit cell is described more fully in Chapter 3, section 3.4.4. The data stream is designed such that 4 valid signals are output simultaneously. Blocks of four pixels are read out serially from the readout with sequencing provided by two multiplexer circuits or "MUXes". One of these MUXes is a "slow" MUX which addresses the 256 rows one by one. The other, "fast" MUX, addresses the columns within each row. The row and column readout multiplexers are implemented as two independent shift register circuits.

The basic integration mode for operating the CRC-744 ROIC is integrate-while-read. In integrate-while-read mode, which can also be thought of as a "rolling wave" mode, the array is continuously integrating even during the read out. Rows are read out and reset sequentially. Once the row reset is complete, the unit cells in a given row begin integrating photocurrent while the other rows are read out. In this mode, all pixels do not integrate simultaneously. The user includes a delay time between frame readouts, so the integration time of a given pixel is equal to the frame readout period plus the delay time. Although pixels in different rows do not begin and end their integration times simultaneously, the total integration time is the same per pixel. Within this integration mode there exist a variety of sampling schemes that can be implemented in the timing, including correlated double sampling (CDS), correlated triple sampling (CTS), sampling up the ramp (SUTR), and multiple or "Fowler" sampling (FS). The timing details for this ROIC are described in more detail in Chapter 3.0.

The overall transfer function of the ROIC is given by

$$\Delta Vout = Asf1*Asf2*\Delta Vin \quad \text{volts} \quad (1)$$

where Asf1 is the gain of the unit cell source follower, Asf2 is the gain of the output stage source follower, and ΔVin is the change in voltage on the unit cell input node. The total gain of the two source followers in the signal path is about 0.8. The transfer function can also be written as

$$\Delta Vout = Zt*\Delta N \quad \text{volts} \quad (2)$$

where Zt is the ROIC transimpedance gain in volts/electron and ΔN is the number of charge carriers collected during the integration time period, including both photo-generated carriers and "leakage" or "dark" current carriers. The transimpedance gain is given by

$$Zt = q*Asf1*Asf2/Cint \quad \text{volts/electron} \quad (3)$$

where q is the electron charge in Coulombs and Cint is the unit cell integration capacitance in Farads. ΔN is given by

$$\Delta N = Cint*\Delta Vin/q \quad \text{electrons} \quad (4)$$

Combining equations (2) and (3), the change in output voltage can be written as:

$$\Delta Vout = q*Asf1*Asf2*\Delta N /Cint \quad \text{volts} \quad (5)$$

Cint is equal to the sum of the detector's capacitance, which is bias dependent, and the stray capacitance of the readout at the input gate to the unit cell source follower. The stray capacitance is dominated by the gate to source capacitance of the source follower. Typical values are 25 fF for the stray capacitance and 30 fF for the InSb detector capacitance with ~ 0.6V bias and 5 fF for the Si:As detector capacitance with ~1.0V bias.

1.3 CRC-744 Design Features and Performance Characteristics

A summary of some of the key design features and performance characteristics for the CRC-744 ROIC are given below in Table 1.1.

Table 1.1. CRC-744 SCA Design and Performance Characteristics.

Parameter	Specification
Pixel Size	30 μm x 30 μm
Array Configuration	256 x 256 or 65,536 elements
Array Active Area	7.68 mm x 7.68 mm
Effective Unit Cell Optical Fill Factor	≥ 98% (Aoptical ≅ 8.8 x 10-6 cm^2)
Number of Outputs	4 + 2 diagnostic + (2 temp sensor)
Clocks (including "switched" biases)	8
Bias/Current Supplies (including "ground")	10/11 (InSb/Si:As) Bias Supplies ; 2 Current Sources 4 detector biases for Si:As; 1 detector bias for InSb
Maximum Frame Rate	≅ 18 Hz
Reset Options	By row, integrate-while-read
IR Detector	InSb or Si:As
Well Capacity	~ 2×10^5 electrons at 0.6 volt reverse bias InSb
	~ 2×10^5 electrons at 1.0 volt reverse bias Si:As
Transimpedance	~ 3 μV/electron at 0.6 volt reverse bias InSb
	~ 5 μV/electron at 1.0 volt reverse bias Si:As
Responsivity Uniformity	< 8% (sigma/mean)
Wavelength Range	Visible to 5 μm InSb; 1-28 μm Si:As
Responsive Quantum Efficiency	≥ 80% peak InSb; ≥ 40% peak Si:As
Operating Temperature	15 - 35 K InSb; 5 - 10 K Si:As
Dark Current	< 1 electron/sec (Si:As @ 6K, InSb @ 15 - 30K)
Noise (input-referred)	~ 6 - 50 mean rms electrons (sampling dependent)
Defective Pixels	typically < 0.5 %

1.4 CRC-744 Architecture and Floor Plan

The CRC-744 Readout Integrated Circuit (ROIC) consists of 256 x 256 pixels (see Figure 1.2). Figure 1.1 illustrates the location of the row "slow" shift register (row MUX) and the column "fast" shift register (column MUX) as well as direction of read out. In this Figure, the first pixel read out, at column #1 and row #1, is located in the lower left hand corner and the last pixel read out, at column #256 and row #256 is located in the upper right hand corner. The readouts "CRC744" logo can be seen with a microscope in the upper left hand corner as oriented in Figure 1.1. Pixels are read out by addressing each row in turn and addressing and reading all columns in each row. Since there are 4 interleaved analog outputs, each output reads out every 4th column, i.e. output #1 reads out columns 1, 5, 9, 13, …, 253; output #2 reads out columns 2, 6, 10, 14, …, 254; output #3 reads out columns 3, 7, 11, 15, …, 255; and output #4 reads out columns 4, 8, 12, 16, …, 256. This readout scheme is repeated 64 times until all pixels in the selected row have been read out, after which the next row is selected.

The CRC-774 ROIC architecture and floor plan is fully illustrated in Figure 1.2. The active array consists of 256 columns and 256 rows. On the periphery of the active array area are the row and column shift registers as well as the two current sources (#1 and #2). At the top of the array in Figure 1.2 are the current source #1 mirror FET (controlled by VGG1 and VSS1) for the unit cell source followers and the clamp circuitry FETs (controlled by VGGCL and VDDCL). Just above the column shift register, but below the active area, are the current source #2 mirror FET (controlled by VGG2 and VSS2) the 64:1 (256:4) column output multiplexer.

Each of the 4 outputs must read out 16,384 pixels. With the fast column clocks running such that the pixel data rate on each output is 250 kHz (4.0 μsec/pixel), the total time required to read out an entire 256 x 256 array is about 66 msec, which corresponds to a 15 Hz frame rate.

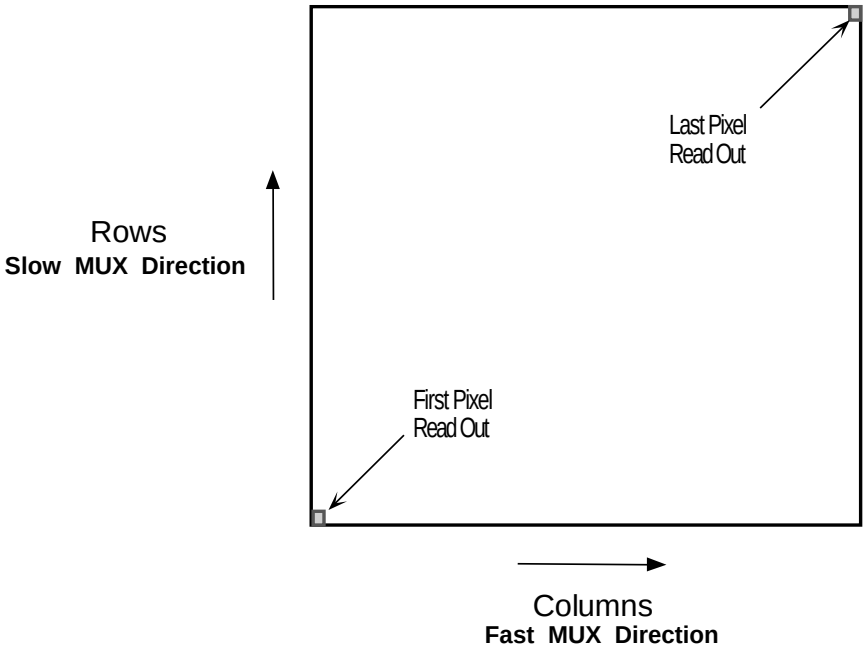
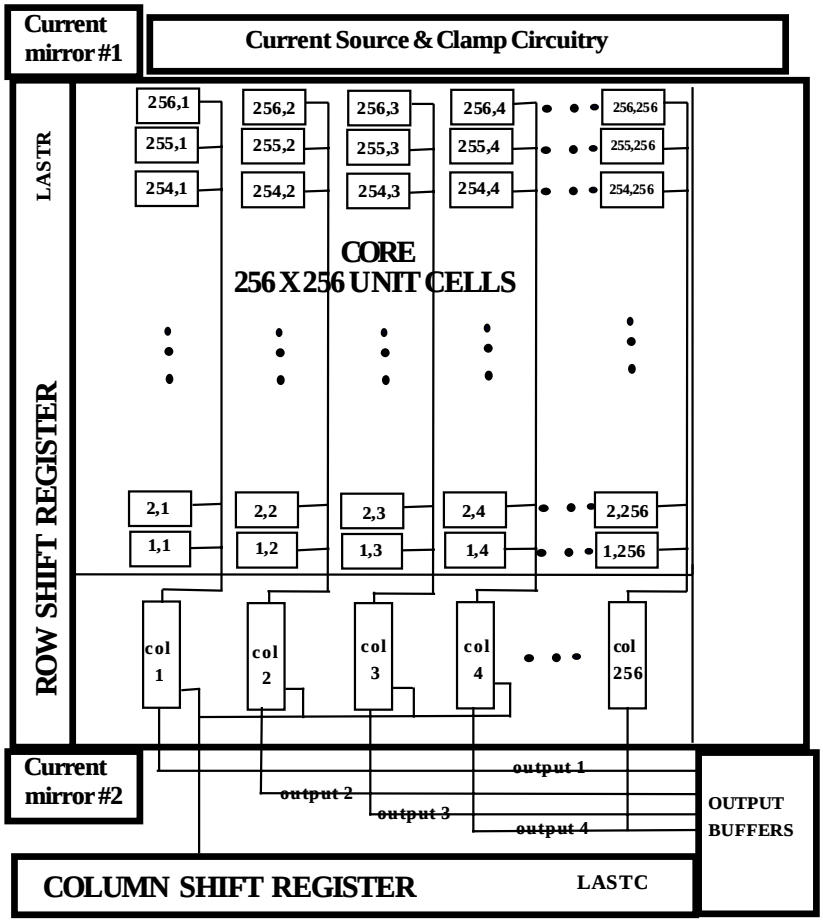


Figure 1.1. CRC-744 Read Out Procession

CRC 744 READOUT



(F) vggcl
(F) vddcl
(F) (vguardl)
(F) (vdetl)
(T) lastr
(F) vssscans
(F) phi1s
(F) phi2s
(F) phisyncs
(F) phirst
(F) phisyncf
(F) phi2f
(F) phi1f
(T) lastc
(F) vsssanf

(F) vsub
(F) vss1
(F) vgg1
(F) vss2
(F) vgg2
(F) vdduc
(F) vrstuc
(F) vdetr
(F) vguardr
(F) vsub
(F) vout1
(F) vout2
(F) vout3
(F) vout4
(F) vddout

(T) Test Pad
(F) Flight or Operational Pad

( ) No longer bonded on LCC

Figure 1.2. CRC-744 ROIC Floor Plan

CHAPTER 2

2.0 CRC-744 ROIC I/O Pad Functions

This chapter provides a description of the CRC-774 ROIC Input/Output (I/O) pad functions and the appropriate bias levels associated with each. It also provides information on the location of the equivalent pad functions on the Leadless Chip Carrier (LCC). Some LCC I/O pads require a series external resistor tied to a DC bias supply (see Figure 3.3). It should be noted that **all external clocks supplied to the CRC-744 are activated (turned on) with a "low" logic level (~ -5 to -7 volts)**.

2.1 ROIC Column Shift Register Clocks ("Fast")

- ØSYNCF: This clock performs synchronization of the fast shift register which controls the column multiplexing functions. It initializes the start pulse for the shift register when the logic level is simultaneously low with Ø2F. Nominal voltage rails are -5.0V (low) and -1.0V(high).
- Ø1F: This clock is the Phase 1 input clock for the fast shift register. Ø1F transitions 32 times per enabled row in a nested fashion with the Ø2F clock. Nominal voltage rails are -5.0V (low) and -1.0V(high).
- Ø2F: This clock is the Phase 2 input clock for the fast shift register. Ø2F transitions 32 times per enabled row in a nested fashion with the Ø1F clock. Nominal voltage rails are -5.0V (low) and -1.0V(high). When both Ø2F and Ø1F are simultaneously low, the shift register is cleared and no columns are addressed.

2.2 ROIC Row Shift Register Clocks ("Slow")

- ØSYNCS: This clock performs synchronization of the slow shift register which controls the row multiplexing functions. It initializes the start pulse for the shift register when simultaneously low with Ø2S. Nominal voltage rails are -7.0V (low) and -1.0V(high).
- Ø1S: This clock is the Phase 1 input clock for the slow shift register. Ø1S transitions 128 times per read in a nested fashion with the Ø2S clock. Nominal voltage rails are -7.0V (low) and -1.0V(high).
- Ø2S: This clock is the Phase 2 input clock for the slow shift register. Ø2S transitions 128 times per read in a nested fashion with the Ø1S clock. When both Ø2F and Ø1F are simultaneously low, the shift register is cleared and no rows are addressed. Nominal voltage rails are -7.0V (low) and -1.0V(high).

2.3 Other ROIC Clocks

- ØRST: This clock performs the row reset function. The supply rail voltages are nominally -5.5 volts (low) and -3.0 volts (high). When a row is selected by either Ø2S or Ø1S and ØRST is set low, all of the 256 detector elements in that row are reset.

2.4 ROIC Switched Biases (Analog)

- VGGCL: This is the bias which is applied to the gate of the clamp MOSFET for each column (see Figure 3.3). This bias and VDDCL control the column bus potential when no row is selected. The nominal bias levels are -5.0 (clamp on) and -1.0 volts

(clamp off). The column clamp transistor should turn on, thereby holding the column bus at a fixed voltage, whenever a transition between rows occurs or during integration without the final row left addressed.

2.5 ROIC DC Biases and Returns

- VSUB: This bias serves as analog ground reference for the CRC-744 ROIC. The nominal bias is 0.0 volts (ground).
- VSS1: This bias is the analog source supply lead for the current mirror circuit for each column line (see Figure 3.3). It is normally set to -1.0 volts to reduce the power consumption of the array. The current mirror supplies the current set by Vgg1 to the unit cells' source follower drivers. Nominally set the current in a unit cell SF between 0.4 -1.0 μA. This will correspond to a current draw of 100 - 250 μA on the Vss1 supply with a single row addressed.
- VSS2: This bias is the analog source supply lead for the auxiliary current mirror circuit for each column output at the output buffer (see Figure 3.3). It is normally not used unless higher data rates are needed. The current mirror supplies the extra current set by VGG2 to the four unit cell source followers connected to the input gates of the output buffer source followers.
- VDDCL: This bias is the clamp voltage for the column bus when no row address is selected (see Figure 3.3). The nominal bias level is between -1.6 to -1.9 volts; this will need to be adjusted depending on the chosen reset level. It should be set to about 0.3V above a threshold above the reset level of the unit cell (i.e., VDDCL ≅ Vreset_level + |Vthreshold| + 0.3V ≅ Vreset_level + 1.6V).
- VDDUC: This bias is the unit cell SFD driver MOSFET drain supply. The nominal bias level is -3.5 volts.
- VRSTUC: This bias is the unit cell SFD (SF1 in Figure 3.3) gate bias that defines the baseline output voltage level with no current. The nominal bias level is -3.5 volts for InSb and -3.2 volts for Si:As.
- VDDOUT: This analog bias is the drain voltage supply applied to the output buffers. Nominal bias level is ~ -1.2 volts, sinking a current of about 160 - 240 μA (40 - 60 μA per output).
- VSSSCANF: This is the source supply for the column ("fast scan") shift register. The nominal bias level is -1.0 volt.
- VSSSCANS: This is the source supply for the row ("slow scan") shift register. The nominal bias level is -1.0 volt.
- VDETCOM or VDET: This bias is the detector common bias, which is connected to the detector backside, the side where the photoflux is incident. The detector applied bias is the difference between VDETCOM and the VRSTUC voltage levels[1]. The

1 The actual bias across the detector is given by Vbias = VDETCOM - VRSTUC - Vzbp, where Vzbp is the "zero bias point.." The zero bias point is an offset shift that naturally occurs when the reset switch, controlled by ØRST, is opened. As the switch opens charge is redistributed resulting in the so called "charge injection effect." The typical zero bias point offset is about +100 mV. This reduces the actual bias across InSb and increases the actual bias across Si:As by this amount.

applied bias level can range from VRSTUC (zero bias) to VRSTUC + Vbias. For InSb set Vbias > 0V and for Si:As set Vbias < 0V. The absolute value of Vbias is the magnitude of the reverse bias across the detector. Typically for InSb, Vbias ≅ 0.6V and for Si:As, Vbias ≅ -1.0V.

- VGUARD: This bias is used only for the IBC detectors and goes to the outer guard ring of the detector array. It is recommended that this bias be set to the reset voltage level, VRSTUC. Its purpose is make the peripheral active pixels "see" the same surrounding electrical environment that the interior active pixels "see."

2.6 ROIC Shift Register Diagnostics

- LASTR: This is a diagnostic output for the row shift register. For diagnostic purposes, a ~10 kΩ resistor should be placed in series between the LASTR output pad and a 0.0 volt bias supply or ground. The test point is the node between the resistor and the LASTR output. The diagnostic pulse will occur after the last row has been successfully clocked. If the slow shift register fails to completely clock all 256 rows the LASTR pulse will not occur. It is recommended that this line be floated when not in use.
- LASTC: This is a diagnostic output for the column shift registers. For diagnostic purposes, a ~10 kW resistor should be placed in series between the LASTC output pad and a 0.0 volt bias supply or ground. The test point is the node between the resistor and the LASTC output. The diagnostic pulse will occur after the last column has been successfully clocked. If the fast shift register fails to completely clock all 256 columns the LASTC pulse will not occur. It is recommended that this line be floated when not in use.

2.7 ROIC Current Sources (Current Mirrors with External Current Control)

- VGG1: This bias provides the current setpoint for the VGG1 current mirror on each of the 256 column bus lines. For current control, a ~400 kΩ metal film resistor must be connected in series with the VGG1 bias. The nominal bias level is ~ -3.0 volts. The ratio of current in VGG1 to a single source follower is 4:1. Nominal current in the unit cell source follower should be ~ 0.4-1.0 μA. The current draw on VGG1 should range between 1.6 and 4.0 μA, the voltage drop across the metal film resistor should range between 0.64 and 1.6 V. With a single row active, the current draw on VSS1 should range between 100 to 256 μA (= 256 x I_{SF} + I_{VGG1}). (See Figure 3.3).
- VGG2: This bias provides the current setpoint for the VGG2 current mirror on the 4 output bus lines. For current control, a ~40 kΩ metal film resistor must be connected in series with the VGG2 bias. This bias is normally not used unless faster pixel settling times are required. The ratio of current in VGG2 to a single bus line is 4:1. So, for example, a desired boost current of 5 μA per output bus line, you should measure a current draw of 20 μA, or a voltage drop across the metal film resistor of 0.8V. With a row and column address active, the current draw on VSS2 should be 40 μA (= 4 x I_{BUS} + I_{VGG2}). (See Figure 3.3).

2.8 ROIC Analog Outputs

- VOUT1,2,3,4: The voltage outputs are connected to the source sides of the four output buffer/driver source followers (SF2 in Figure 3.3). To function properly, each output requires a ~30 kW metal film load resistor to a bias (~ +1V) to provide the necessary current to the SF. Nominal drain to source current should be 40 - 60μA per output buffer.

2.9 ROIC Internally Generated Clocks

- COLEN: This internal clock controls the sequence of 4 outputs that are placed onto the output bus lines from the 256 column bus lines (see Figure 3.3). It is generated from the column address bit and the Ø1F and Ø2F column shift register clocks. This clock is transparent to the user, i.e. nothing needs to be done provided the proper timing of the column shift register clocks is provided.
- ROWEN: This internal clock controls the sequence of rows that are placed, one at a time, onto the 256 column bus lines (see Figure 3.3). It is generated from the row address bit and the Ø1S and Ø2S row shift register clocks. This clock is transparent to the user, i.e. nothing needs to be done provided the proper timing of the row shift register clocks is provided.

Table 2.1. CRC-744 ROIC and LCC Pad Description

Pad #	Name	Function	Nominal Level	Pad Type
1	VSUB	Substrate contact	0.0 V	Bias
2	VGGCL	Column clamp gate bias	-5.0/-1.0 V	Switched bias
3	VDDCL	Column clamp bias	~ -1.9 to -1.6 V	Bias
6	LASTR	Last row diagnostic tap	10kΩ to 0V	Output
7	VSSSCANS	Source supply for the slow shift register	-1.0 V	Bias
8	Ø1S	Phase 1 clock for the slow shift register	-7.0/-1.0 V	Clock
9	Ø2S	Phase 2 clock for the slow shift register	-7.0/-1.0 V	Clock
10	ØSYNCS	Sync clock for the slow shift register	-7.0/-1.0 V	Clock
11	ØRST	Reset clock	-5.5/(-3.2 to -3.5)V	Clock
12	ØSYNCF	Sync clock for the fast shift register	-5.0/-1.0 V	Clock
13	Ø2F	Phase 2 clock for the fast shift register	-5.0/-1.0 V	Clock
14	Ø1F	Phase 1 clock for the fast shift register	-5.0/-1.0 V	Clock
15	LASTC	Last column diagnostic tap	10kΩ to 0V	Output
16	VSSSCANF	Source supply for the fast shift register	-1.0 V	Bias
36	VDDOUT	Drain supply for the output buffer rail	-1.2 V	Bias
37	VOUT 4	Output 4	~30 kΩ to 0-1V (40-60µA)	Output
38	VOUT 3	Output 3	~30 kΩ to 0-1V (40-60µA)	Output
39	VOUT 2	Output 2	~30 kΩ to 0-1V (40-60µA)	Output
40	VOUT1	Output 1	~30 kΩ to 0-1V (40-60µA)	Output
41	VSUB	Substrate contact	0.0 V	Bias
42	VGUARD	Peripheral guard ring for Si:As detector	VRSTUC(Si:As) / float (InSb)	Bias
43	VDETCOM	Detector backside bias	variable	Bias
44	VRSTUC	Unit cell source follower gate reset bias	-3.5 (InSb)/ -3.2 (Si:As)	Bias
45	VDDUC	Unit cell drain bias rail	-3.5 V	Bias
46	VGG2	Control for setting supplemental current source	~ 0.16-0.48 mA	Bias
47	VSS2	Supplemental current source bias rail	0.16 to 1.6 V (~40kΩ series R)	Bias
48	VGG1	Control for setting unit cell current source	0.64 to 1.6 V (~400kΩ series R)	Bias
49	VSS1	Unit cell source bias rail	-1.0 V	Bias
51	VSUB	Substrate contact	0.0 V	Bias

CHAPTER 3

3.0 OPERATIONAL AND TIMING REQUIREMENTS

3.1 Integration and Reset

In integrate-while-read mode, one row is addressed, read out, and reset while the other 255 rows integrate. The next row is then addressed, read out, and reset as the other 255 rows integrate. When this process has cycled through all 256 rows, it simply restarts at the first row after some user defined delay time. The integration time for a given pixel is the time from one address, read, and reset cycle to the next, i.e. the frame readout time plus the user defined delay time. The sequential addressing of rows to read out is controlled by the operation of the row shift register. The sequential resetting of rows is controlled by the row shift register in conjunction with the ØRST clock. Although pixels in different rows do not begin and end their integration times simultaneously, the total integration time is the same per pixel.

By not resetting the rows during a readout, the user can implement various multiple sampling techniques, such as sampling up the ramp and Fowler sampling. These methods allow the user to reduce the readout noise substantially by a factor ~$1/\sqrt{(Ns)}$, where Ns is the number of samples. This technique works until a lower noise floor is reached, beyond which the noise will not improve. An excellent review article on the operation of the CRC-744 readout can be found in "Development of infrared focal plane arrays for space," Jian Wu et. al, Rev. Sci. Instrum. 68 (9), September 1997.

3.2 Timing Requirements for the Column (Fast) Clocks

The column clocks are:

- ØSyncF - Synchronizing clock for the column shift register
- Ø1F - Phase 1 input clock for the column shift register
- Ø2F - Phase 2 input clock for the column shift register
- COLEN - Internally generated clock that transfers ("enables") a particular column block of four outputs from the 256 column bus lines to the 4 column output lines (see Figure 3.3)

The propagation of the initial ØSyncF pulse along the column shift register is controlled by the frequencies of the Ø1F and Ø2F clocks. The ØSyncF clock must be clocked once every row. The Ø1F and Ø2F clocks must be symmetrically nested for the proper propagation of the column address bit (initially injected by the ØSyncF pulse) needed for read out. In other words, it is important that the Ø1F and Ø2F clocks are never simultaneously active (logic level 0, corresponding to -5V). Proper operation is achieved by adjusting the duty cycles of the Ø1F and Ø2F clocks so that the clocks are active low for ~40% of the pixel readout cycle and inactive high for ~60% of the pixel readout cycle. Figure 3.1 shows the recommended nesting sequence for the column clocks.

Windowing in the column direction is possible by bursting the address bit through the column shift register to the desired starting column, slowing down, reading out the columns within the window, and bursting the address bit to the end of the shift register.

The following summary of requirements apply to the ØSyncF, Ø1F,and Ø2F fast clocks:

- Active clocks are at the most negative clock supply rail, i.e. **active low**
- The fast shift register start bit is loaded when ØSyncF and Ø2F are simultaneously active low
- ØSyncF needs to remain active low longer than Ø2F to enable the fast shift register start bit
- Ø2F and Ø1F edges must not overlap and must not be active simultaneously for proper clocking
- When Ø2F and Ø1F are both active simultaneously the column shift register is cleared
- Maximum clock speed for the fast shift register under nominal (non-bursting) operating conditions is about 3 µsec per pixel (2.9 µsec active, 3.1 µsec inactive nested pair). We typically operate at 5 µsec per pixel.
- It is not recommended to set the column clock active level more negative than -5.5V; -5.0V is the recommended operating level

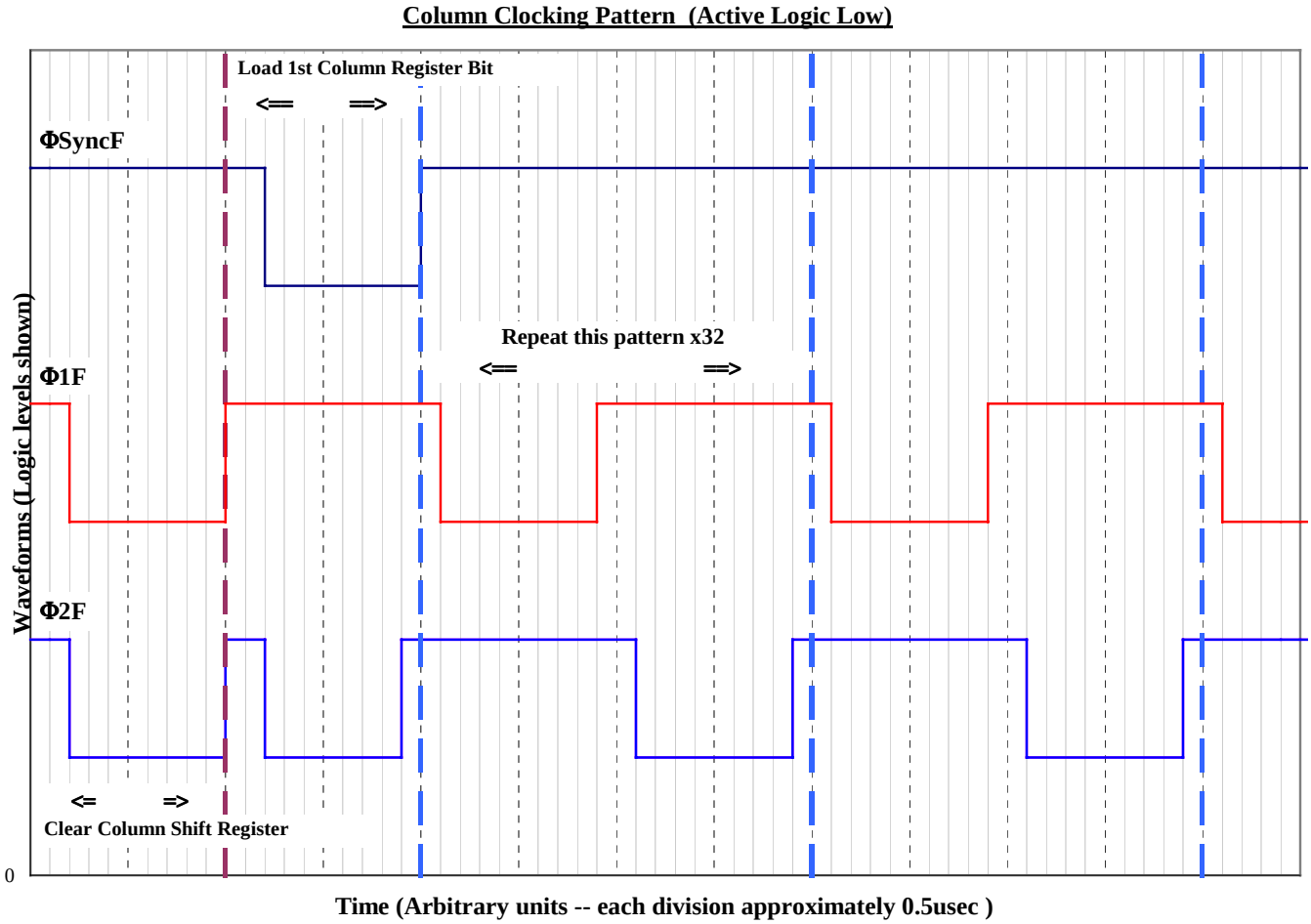


Figure 3.1. CRC-744 ROIC Column Clock Timing

3.3 Timing Requirements for the Row (Slow) Clocks

The row clocks are:

- ØSyncS - Synchronizing clock for the row shift register
- Ø1S - Phase 1 input clock for the row shift register
- Ø2S - Phase 2 input clock for the row shift register
- ROWEN - Internally generated clock that transfers ("enables") a particular row of the array onto the 256 column bus lines (see Figure 3.3)

The propagation of the ØsyncS pulse along the row enable shift register is controlled by the frequencies of the Ø1S and Ø2S clocks. As with the column clocks, it is important that the row clocks be properly nested for the proper propagation of the row address bit (initially injected by the ØSyncS pulse) needed for read out. In normal operation, the row clocks must never be simultaneously active (logic level 0, corresponding to -7V).

Again, windowing in the row direction is also possible by "bursting" the address bit through the row shift register to the desired row, slowing down, reading out the desired rows (window), and bursting the address bit to the end of the row shift register.

The following summary of requirements apply to the ØSyncS, Ø1S,and Ø2S slow clocks:

- Active clocks are at the most negative clock supply rail, i.e. **active low**
- The slow shift register start bit is loaded when ØSyncS and Ø2S are simultaneously active low
- ØSyncS needs to remain active low longer than Ø2S to enable the slow shift register start bit
- Ø2S and Ø1S edges must not overlap and must not be active simultaneously for proper clocking
- When Ø2S and Ø1S are both active simultaneously the row shift register is cleared
- A delay of ~3 μsec is sufficient time to clear the address registers (see figures below)
- A delay following a row transition of ~10 μsec is recommended for settling considerations
- It is not recommended to set the row clock active level more negative than -7.0V or less negative than -6.0V; -7.0V is the recommended operating level
- We recommend that the operation of the row clocks follow the general pattern shown in Figure 3.2. We prefer to keep the last row addressed after readout. This keeps the current flowing through a given row of unit cell source followers. This provides thermal stability and reduces transients in the operation of the array.

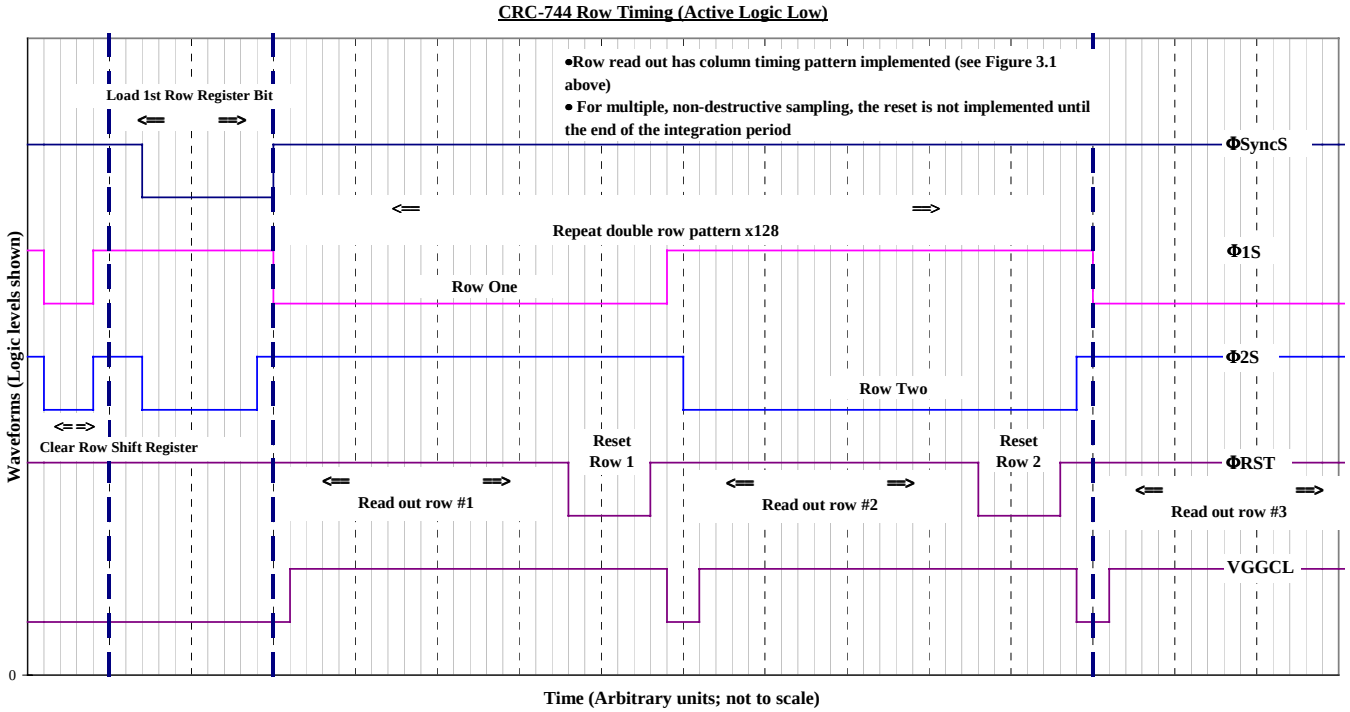


Figure 3.2. CRC-744 ROIC Row Clock Timing

3.4 Timing Requirements for the Signal Chain Clocks

3.4.1 Basic Operation of the Signal Chain

To fully understand the readout, it is important to understand the basic operation of the signal chain.

Photocurrent and dark or "leakage" current from the detector integrates onto the unit cell integration capacitance whenever the row reset switch is inactive (open, gate logic HIGH). The direction of integration is dependent on the type of detector array that is hybridized to the readout. Typically the reset level is initially set to about -3.5V for InSb and -3.2V for Si:As and the signal at full capacity integrates up to -2.9V for InSb biased 0.6V and down to -4.2V for Si:As biased 1V. When the row enable (ROWEN) FET is activated for some selected row, then the current source defined by VGG1 is active. The ROWEN clock is an internally generated clock from the row clocks Ø1S and Ø2S and the row address bit. When activated, a particular row of source follower outputs is transferred to the 256 line column bus. At this stage, the clamp switch FET controlled by the gate level VGGCL should be inactive (open, gate logic HIGH). Hence, the source of the unit cell source-followers (SF1 in Figure 3.3) will follow the signal swing, reduced by the SF1 gain, ASF1 ≅ 0.9, and more positive by a threshold voltage drop ≅ 1.3V. For example, if the reset voltage is at -3.2V and the voltage swing due to integrated signal is +0.5V, the voltage at the source side of SF1 will go from ~ -1.9V at reset (-3.2V + 1.3V) to -1.45V with the integrated signal (-1.9V + A_{SF1}x ΔVsig).

Following row selection and activation, the internal column enable (COLEN) FET is activated. The COLEN clock is an internally generated clock from the column clocks Ø1F and Ø2F and the column address bit. Once activated, four adjacent pixels in the selected row have

their signal levels transferred from the column bus to the output bus that feeds the gates of the four source follower output buffers (SF2 in Figure 3.3). The source side of each source follower output buffer will follow the signal level, reduced by the SF2 gain, ASF2 ≅ 0.9, and more positive by the threshold drop ≅ 1.3V. Hence, the output of the source-follower (VOUT) will swing from ~ -0.6V at reset (-3.2V + 1.3V + 1.3V) to -0.2V with the integrated signal (V_{OUT} = -0.6V + A_{SF1}x A_{SF2}x ΔVsig).

After a selected row has read out all columns, the row is reset by activating ØRST (logic LOW), which feeds the gate of the row reset FET. When the reset switch is deactivated (logic HIGH) the integration time starts again on this row. This sequence continues until all the rows have been read out. A user defined delay time allows the integration time to vary from a minimum time equal to the frame readout period to an arbitrarily long time equal to the frame readout period plus the user defined delay time.

3.4.2 The Signal Chain Clocks

The signal chain clocks are:

- COLEN - This internally generated clock is described under the column clocks.
- ROWEN - This internally generated clock is described under the column clocks.
- ØRST - This clock controls application of the reset voltage level, VRSTUC, to the integration capacitor. This voltage is used to set the baseline level at the gate input to the unit cell source follower (SF1). It is applied , on a row by row basis, following the readout of the row. For “non-destructive” readout, the reset is not applied for several frame readout periods. This allows the user to implement other sampling techniques such as sampling up the ramp or multiple (“Fowler”) sampling.
- VGGCL - This switch bias controls the gate to a “clamp” circuit switch. See the discussion of the clamp circuit in section 3.4.3 below, “The VGGCL Clamp Circuit.”

3.4.3 The VGGCL Clamp Circuit

It is highly recommended that the user implement the “clamp” circuitry located on the column bus just below the unit cell source followers and controlled by the VGGCL gate. If you do not perform the "clamping", then the source node of the unit cell source follower FET will be pulled up to the VSS1 level (-1V) whenever you are not addressing a row. This “collapses” the column bus lines to VSS1 putting a strain on the system to quickly recover when the row is enabled. It will lead to transient effects for fast operation. In general, for readouts operating very cold, you want to minimize any unnecessary large excursion swings of the FET levels.

There is an additional “option” that avoids the necessity of using the VGGCL circuit. Below I describe the two options that the user can utilize to stabilize the source node of the unit cell source followers when the array is not being readout.

Option 1: Set VDDCL @ -2.0V nominal (the desired “clamp” level), and toggle VGGCL between -5V (active clamping) and 0V (inactive). Activate VGGCL (logic LOW) whenever a row is not addressed and during row clock transitions. VGGCL activation is essentially determined by the logical NAND of Ø2S with Ø1S. This option is routinely used in our own test labs. This is the “standard” use of the clamp circuitry.

Option 2: VGGCL and VDDCL can be unused if the array is always left addressed, even during integration (i.e., the user defined delay time). This technique, which leaves the last row addressed maintains the current flow in the SF1 output (column bus) line and thus prevents the node from being pulled up to VSS1. This has the added advantage of providing greater thermal stability since the current source is not cycled on and off during readout and integration, respectively. The disadvantage is that the detectors in the last row will pick up the "glow" associated with this current in the unit cell source-follower; however, experience shows this is often a preferable trade-off for improved overall stability. This option is used by the "SIRTF" (Space Infrared Telescope Facility) space mission.

In this mode, the VGGCL is not activated during the row clock transitions. Clock switching should probably not occur faster than ~200 nsec, but should be at ~200 nsec to prevent the column bus line from "collapsing" to VSS1 before the next row is activated.

3.4.4 The Unit Cell SFD Input Circuit

The unit cell of the CRC-744 ROIC contains only three transistors (see Figure 3.3). The heart of the unit cell Source Follower per Detector (SFD) input circuit consists of a single PMOS driver transistor which operates as a source follower. The SFD is ideally suited to very small unit cells and offers low noise with near unity gain. The other two transistors in the unit cell function as switches which are controlled by on-chip clocks. The "reset" switch FET allows the input node to the detector to be reset to a well defined bias (VRSTUC) at the beginning of each new frame. The gate of the reset FET is connected to the ØRST (reset) clock which is activated by the internal ROWEN clock. The "row enable" switch FET, whose gate is also controlled by the ROWEN clock allows the source follower in all unit cell to turn on by connecting the drain of the unit cell source follower to the power rail VDDUC. Once a row has been activated, the current is supplied by the current mirror controlled by VGG1. This load current must be large enough to drive, or slew, the capacitance Cmux of the common output bus. Because the load MOSFET for the SFD is outside the unit cell, there is no power dissipation in the unit cell until the unit cell is "enabled" by the ROWEN via the row shift register.

3.5 Shift Register Diagnostic Outputs

The LASTR and LASTC diagnostic outputs are voltage taps which serve as diagnostic outputs for verification of proper shift register operation. The LASTR diagnostic output verifies that the row shift register is working properly out to the last row (row 256). Similarly, the LASTC diagnostic output verifies that the column shift register is working properly out to the last column (column 256). To verify correct operation, a digital voltage pulse is detected on these outputs when the last row or column is addressed.

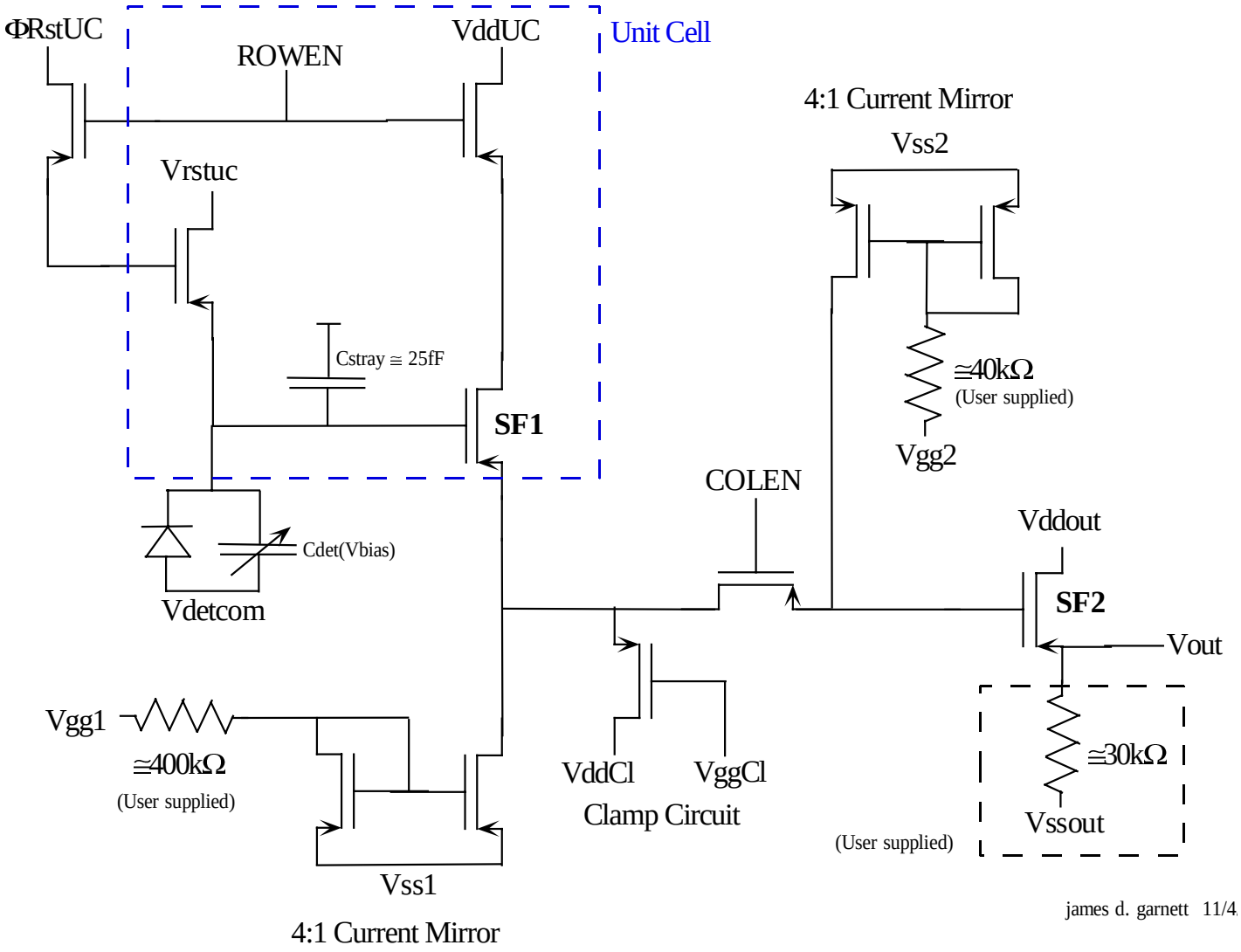


Figure 3.3. CRC-744 Readout Signal Chain

APPENDIX A
GENERAL SAFETY PROCEDURES & BONDING DIAGRAMS

A.1 General Handling and Storage Procedures

Note: The SCAs are static sensitive. Static protection must be observed during handling. Wearing a grounded wrist strap and a static-safe smock at an ESD safe workbench is highly recommended.

Because the SCAs are static sensitive, static-safe procedures should be used during handling and storage. While handling the SCA, a grounded wrist strap should be used to prevent build up of static charge. During temporary storage in a laboratory environment, SCA/LCCs should be placed inside a "recloseable" static shielding bag such as the 3M 2110R bag. For long-term storage, one of the following methods should be used:

1. Store SCA/LCC in an evacuated bell jar.
2. Store SCA/LCC in a hermetically sealed "dry" box which is continuously purged with a dry inert gas such as dry N_2. This method is almost as good as storage under vacuum but allows easier access to the parts in storage.
3. Store SCA/LCC in a static-safe hermetic package with a desiccant to remove water vapor.

A.2 Power Up Sequence

All external connectors to your infrared dewar should have grounding caps in place prior to mounting your SCA inside the dewar. Only handle the SCA when you are grounded with a wrist strap. After the SCA is mounted into your mating socket inside your dewar, you should disconnect the grounding caps on your external connectors and attach your cables with no power applied. First bring up the biases, preferably all to ground, and then subsequently to their nominal operating voltage levels. Only after the biases are applied should you bring up the clocking levels. When shutting off your system, first shut off the clocks and then turn off the bias levels. Remove the cables and attach the grounding caps. The grounding caps should remain in place as long as the SCA is contained in the dewar and is not powered up.

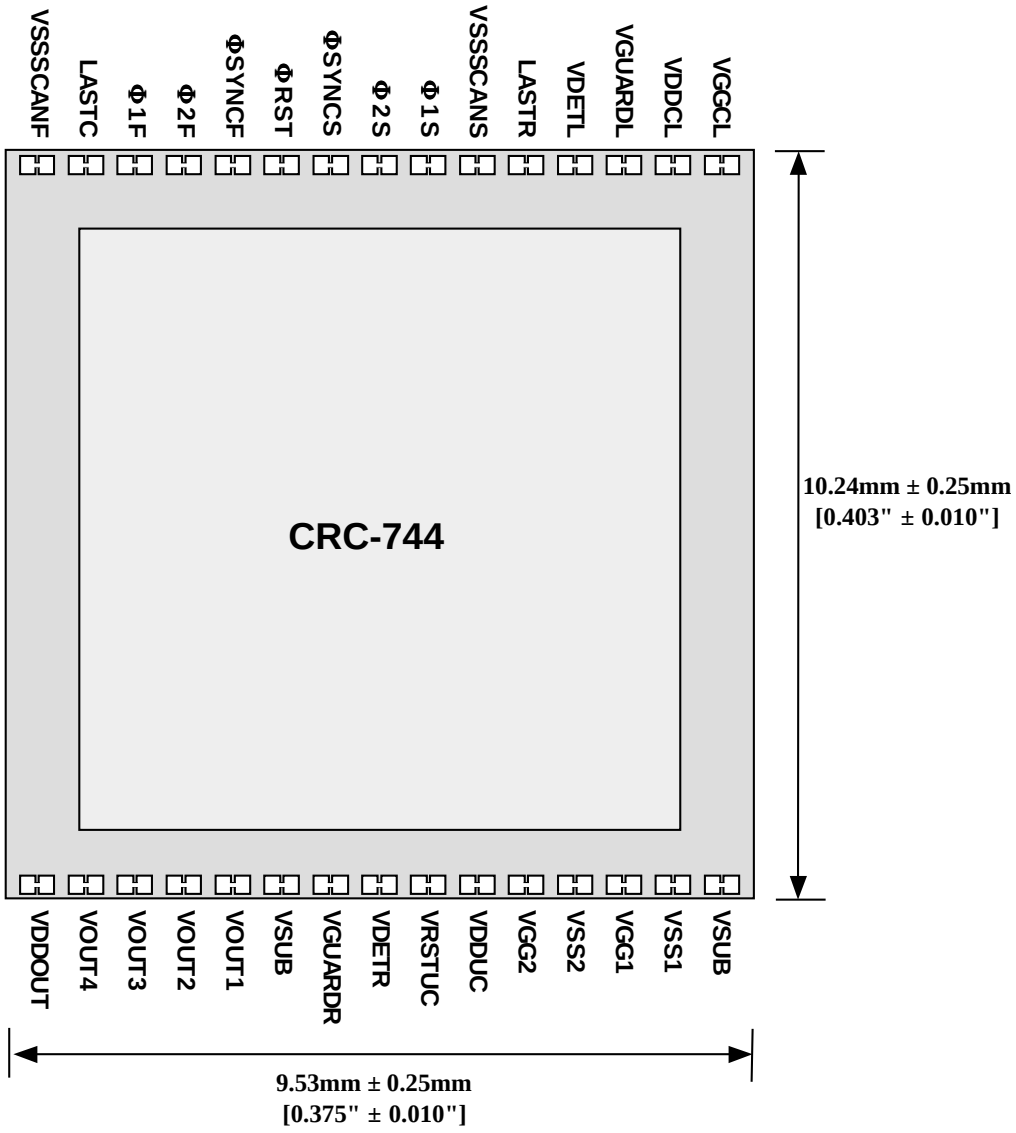


Figure A.1. 256 x 256 CRC-744 ROIC Bond Pad Functions

NOTE: There are a total of 27 input/output bond pads (excluding VGUARDL, which is no longer bonded, the second VSUB, and VDETL, which is not independent of VDETR), including 4 analog outputs, 2 diagnostic outputs, 7 clocks + 1 “switched” bias, and 13 bias supplies.

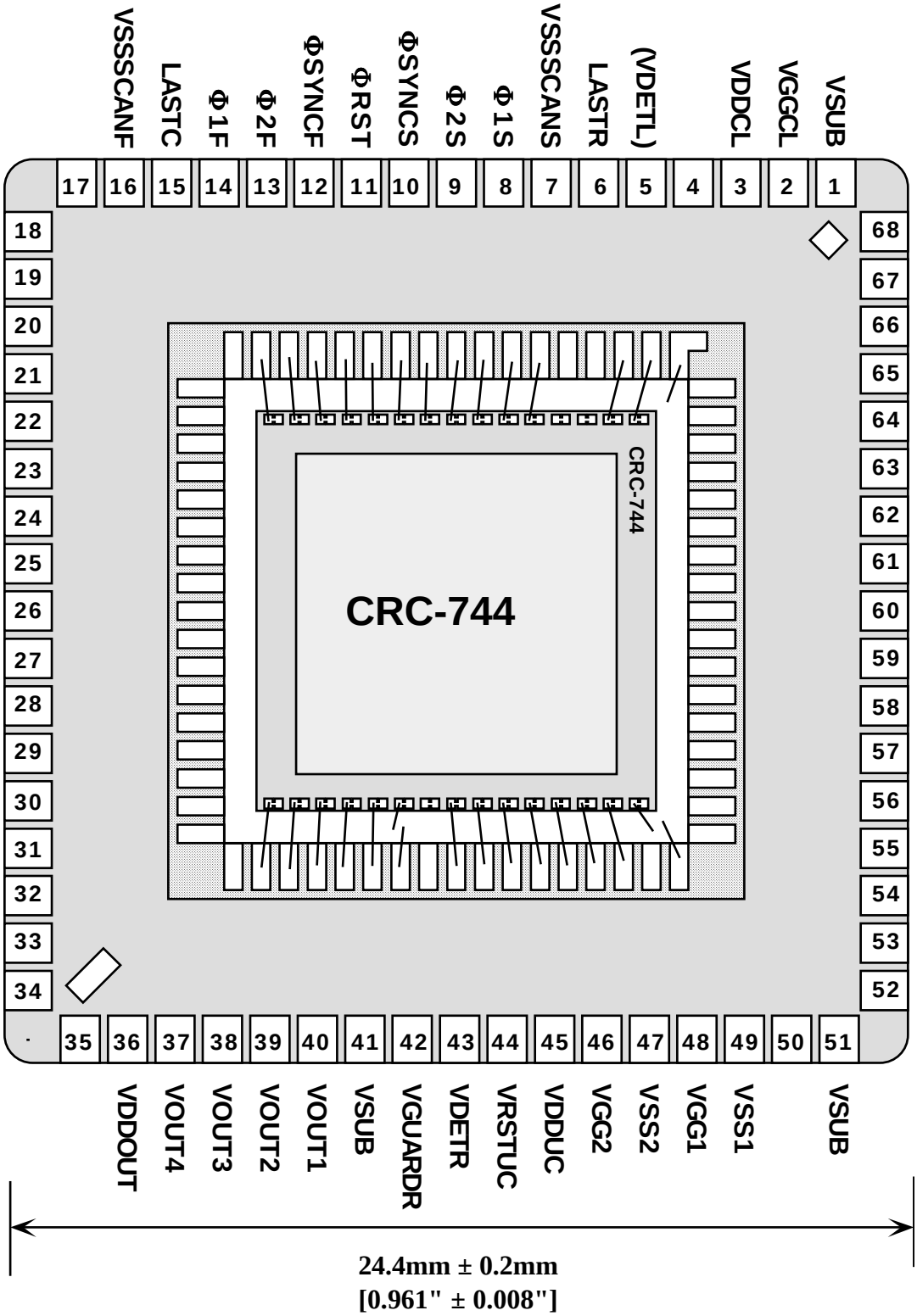


Figure A.2. CRC-744 Bonding Diagram for the 68-pin LCC

CRC-463 GENERAL DESCRIPTION

12/20/90

The CRC-463 is a PMOS multiplexer chip designed to interface with a 256 by 256 detector array. Detectors are spaced 30 μm center-to-center in both dimensions and self-integrate on their own capacitance.

Physical Layout

The CRC-463 reads sequentially starting in the lower left corner in Figure 1. There are four output amplifiers, each reading out every fourth column, e.g., output 1 reads out columns 1, 5, 9, etc. The unit cell readout schematic is shown in Figure 4.

Packaging and Bonding

The CRC-463 is mounted in a 68-pin carrier as shown in Figure 2. Note that Vsub, Vdet gate, and Vdet are each brought out on two pads. These pairs can be shorted together in the dewar. Since Vgg is the only lead that does not have diode static protection, a 15 volt Zener diode to ground is recommended for Vgg and can be used for additional static protection on other pads. (Note: all chip voltages are negative.)

Electrical Settings

Typical voltage levels for the clocks and biases are shown in Table A. For each output we currently use a 10 kΩ resistor to ground as the load. (For frame rates faster than 4 Hz, either connecting the resistor to a positive supply or replacing it with a 200 μA current source may be required.) Pads labeled Last R and Last C are for diagnostic purposes only: they may be connected by a 10 kΩ resistor to -6 volts to observe the pulse that has propagated down the Row and Column scanner, respectively.

Timing

A timing pattern for reading out the CRC-463 in a correlated double or triple sampling mode is defined in Table B with the waveforms shown in Figure 3. The pattern starts with a frame start pulse and a logical "1" is latched into the slow (row) scanner (subpatterns 1 and 3). Then the first row in enabled and a "1" is latched into the fast (column) scanner (SP 5). Next the "1" is shifted through the 64 "bits" of the fast scanner. A given fast scanner bit reads a detector signal onto each of the 4 output amplifiers (256/4 = 64). When the second row is enabled, other subpatterns (SP7 and 8) are required to read out the row since the ϕ1 slow and ϕ2 slow voltages are reversed from row 1 levels. Subpatterns 5, 6, 7 and 8 are repeated 128 times to read out the entire array.

Subarray readouts of the CRC-463 are possible. The row and column scanners are shifted to the desired starting position; readout of the subarray is performed with normal clocking; then the scanner "1" bit is zeroed by turning both ϕ1 and ϕ2 ON at the same time. (Normally, ϕ1 and ϕ2 are non-overlapping, complementary clocks.) This technique has been demonstrated in the test lab at SBRC.

Nondestructive reads have also been demonstrated with the CRC-463. This is accomplished by resetting ϕrst normally during one frame and then not resetting (ϕrst = -3v.) on subsequent frames.

TABLE A: TYPICAL CRC-463 CLOCK AND BIAS LEVELS

Biases

Function	Voltage
Vss	0.0 (Ground)
Vgg	-1.5
Vdd out	-1.0
V3	-2.8
Vdduc	-3.2
Vdet	Vdduc + (0.2 to 0.8)
Vdet gate	Vdet - (1.5 to 2.0)
Vsub	0.0 (Ground)

Clocks

Function	Voltage Rails
ϕsync slow	-3 to -7
ϕ1 slow	-3 to -7
ϕ2 slow	-3 to -7
ϕsync fast	-3 to -7
ϕ1 fast	-3 to -7
ϕ2 fast	-3 to -7
ϕrst	-3 to -6.2

TABLE B: CRC-463 CORRELATED TRIPLE SAMPLING TIMING

Subpattern (SP) Definitions

SP #	Starting Address	Length (BITS)	Purpose	Frequency
1	1	16	Frame start pulse	1/frame
3	29	24	Start slow (row) scanner	1/frame
5	73	24	Start fast scanner/row shift (odd rows)	128/frame (1/odd row)
6	97	48	Readout one odd-numbered row	32/row
7	145	24	Start fast scanner/row shift (even rows)	128/frame (1/even row)
8	169	48	Readout one even-numbered row	32/row
9	217	100	Dead time for integration	1/frame

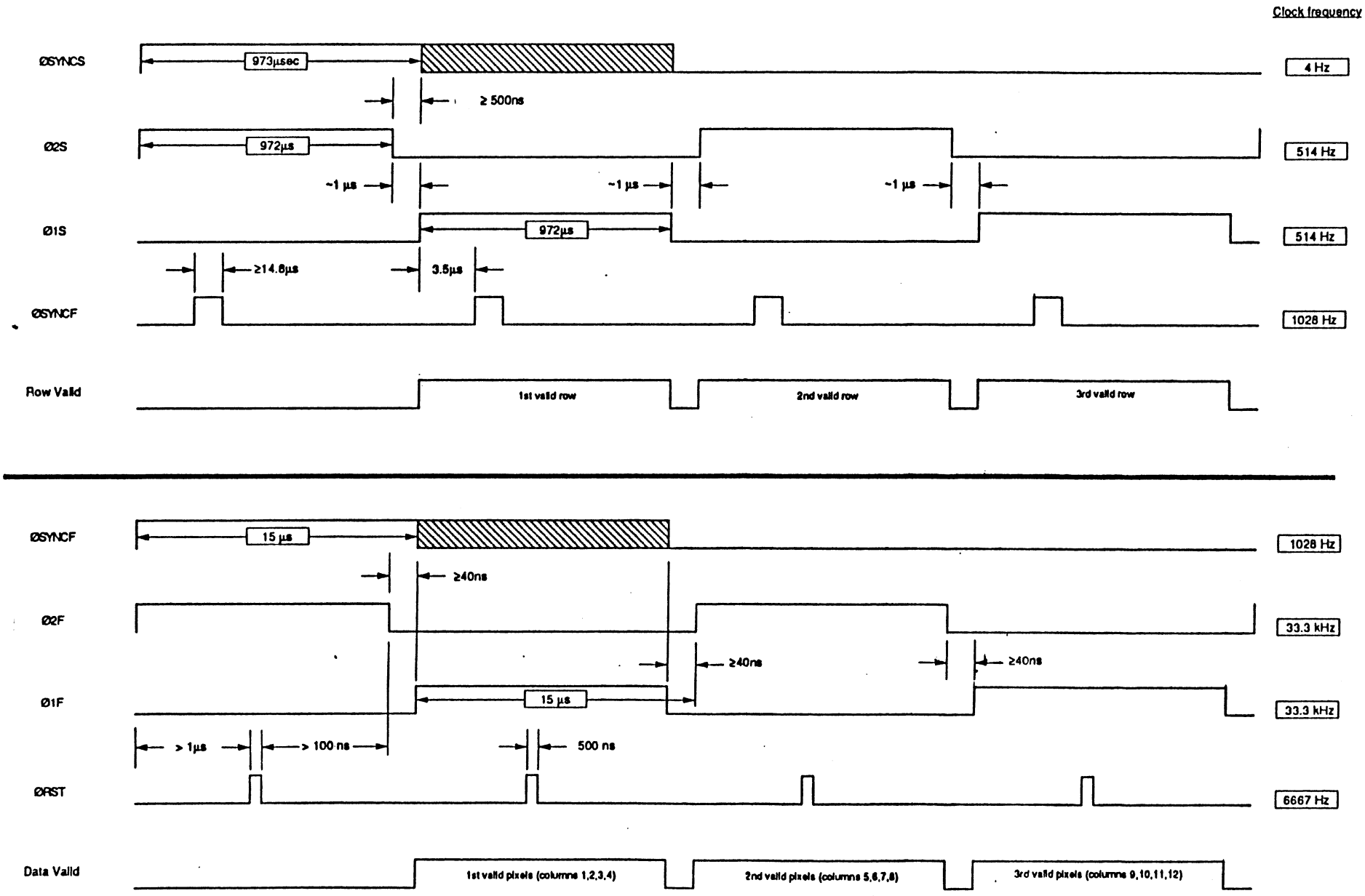
(NOTE: SP 2 and 4 are unused dead times)

Sequence:

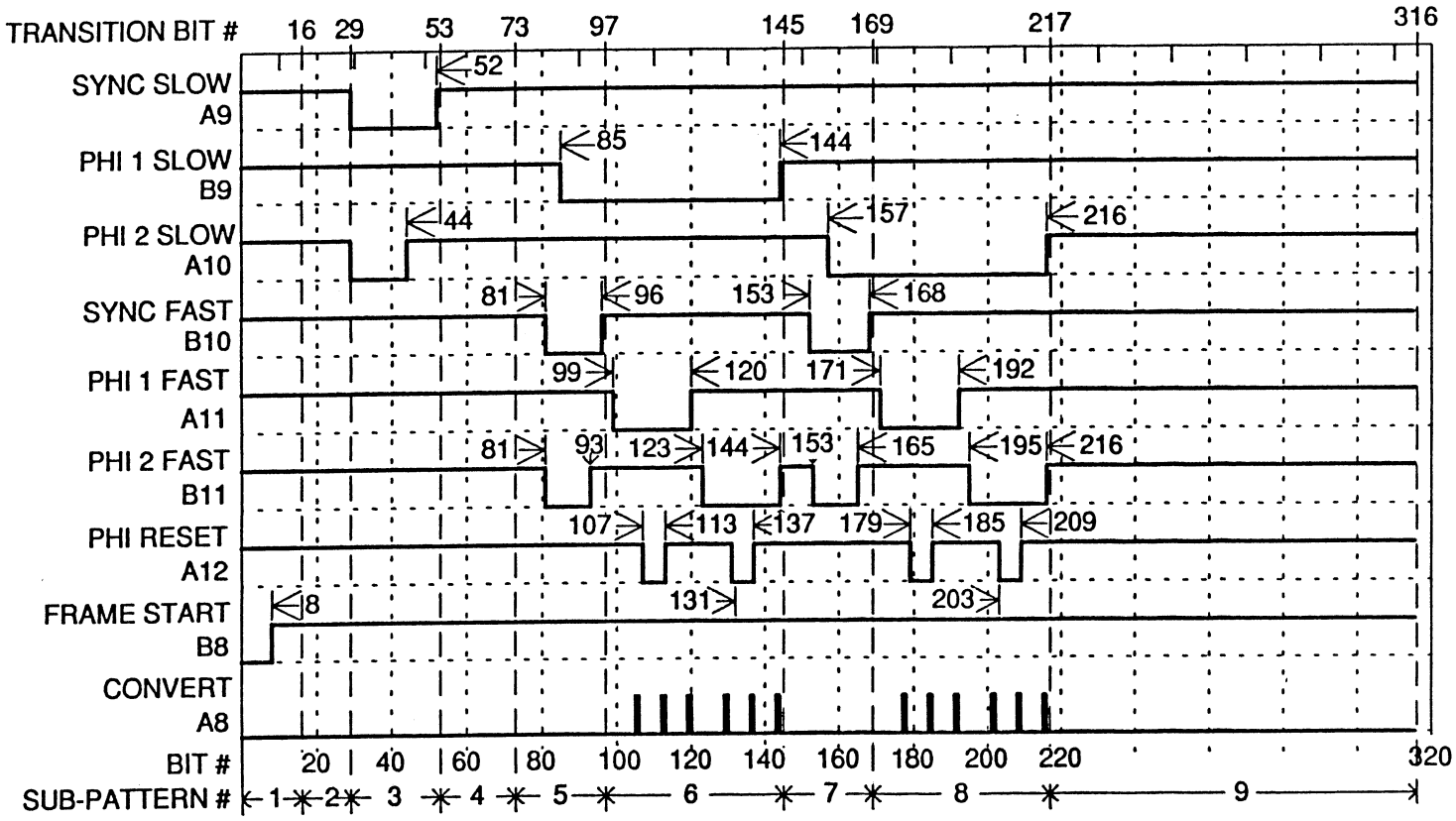
SP1
SP3
SP5
SP6 Repeat 32 times } Repeat SP 5, SP6, SP7, and SP8 a total of 128 times.
SP7 {
SP8 Repeat 32 times }
SP9 Repeated as needed for total integration time

CRC-463 Timing Diagram

(Blocked numbers assume 4Hz operation. All others constant.)



CRC 463 TIMING SUB-PATTERNS



CONVERT A8 HIGH BIT #

105 & 106
112 & 113
119 & 120
129 & 130
136 & 137
143 & 144
177 & 178
184 & 185
191 & 192
201 & 202
208 & 209
215 & 216

FIGURE 3

12/20/90

CRC-463 PHYSICAL LAYOUT

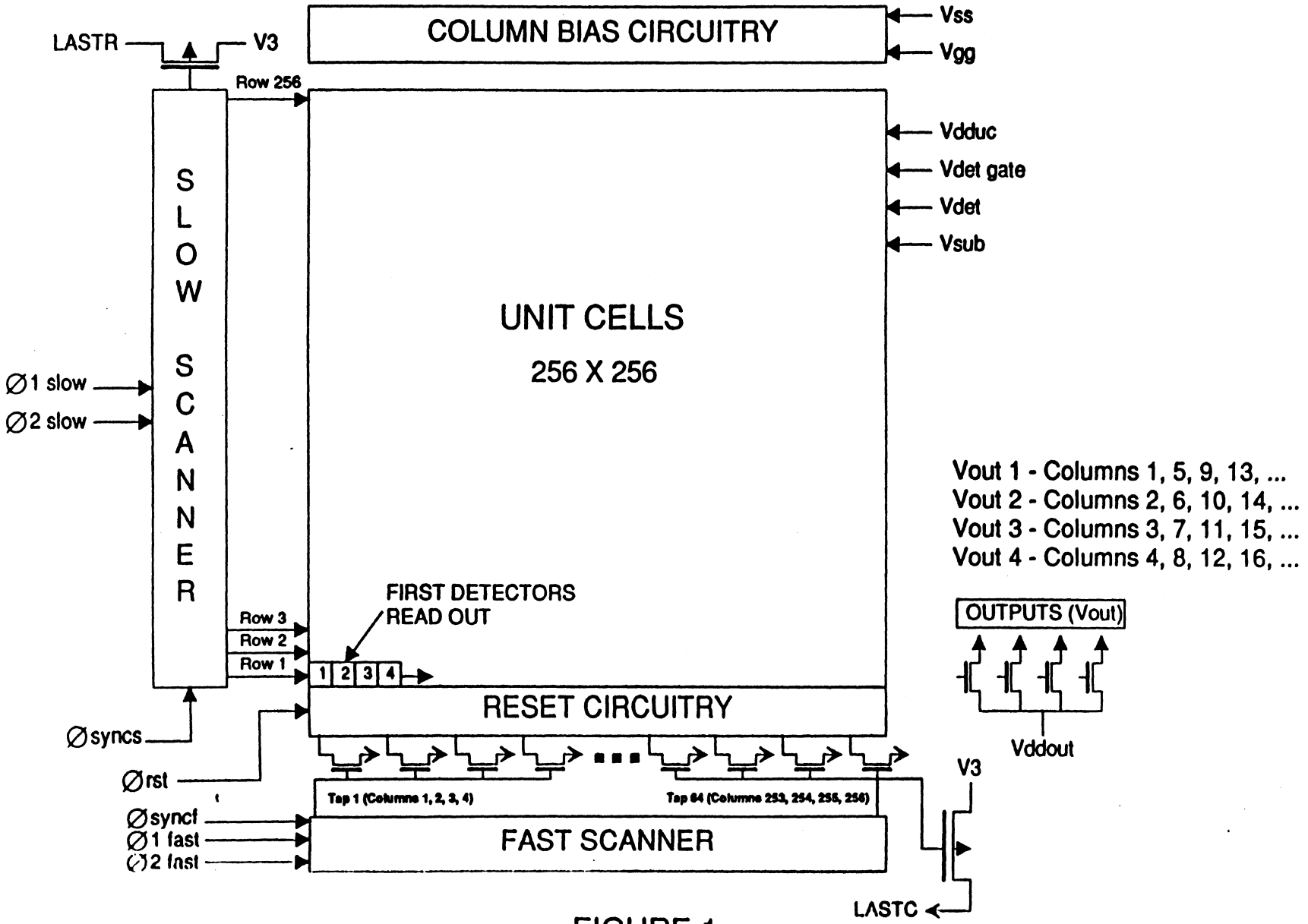
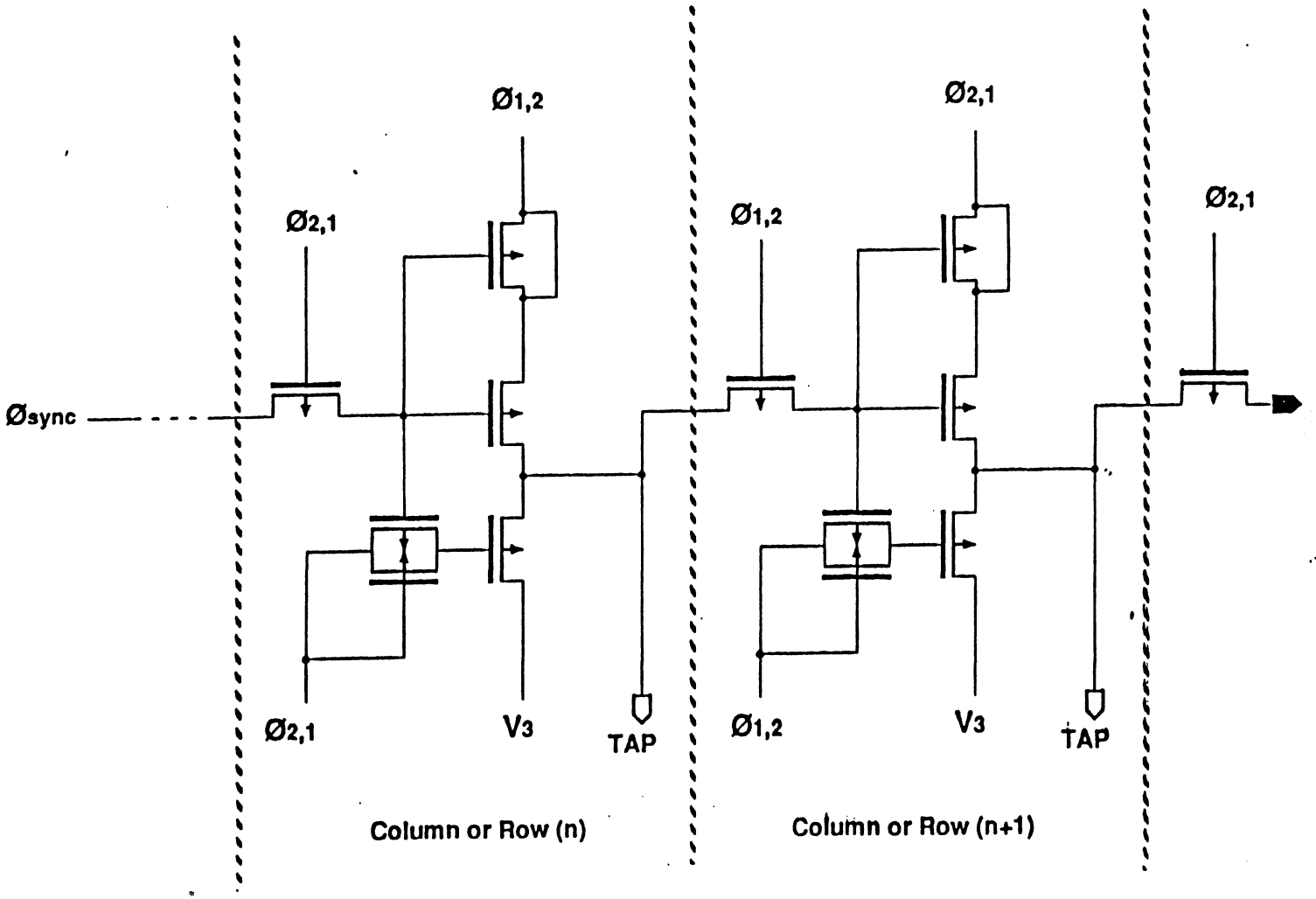


FIGURE 1

12/20/90

CRC-365, CRC-463 READOUT SCANNERS



CRC-463 UNIT CELL READOUT SCHEMATIC

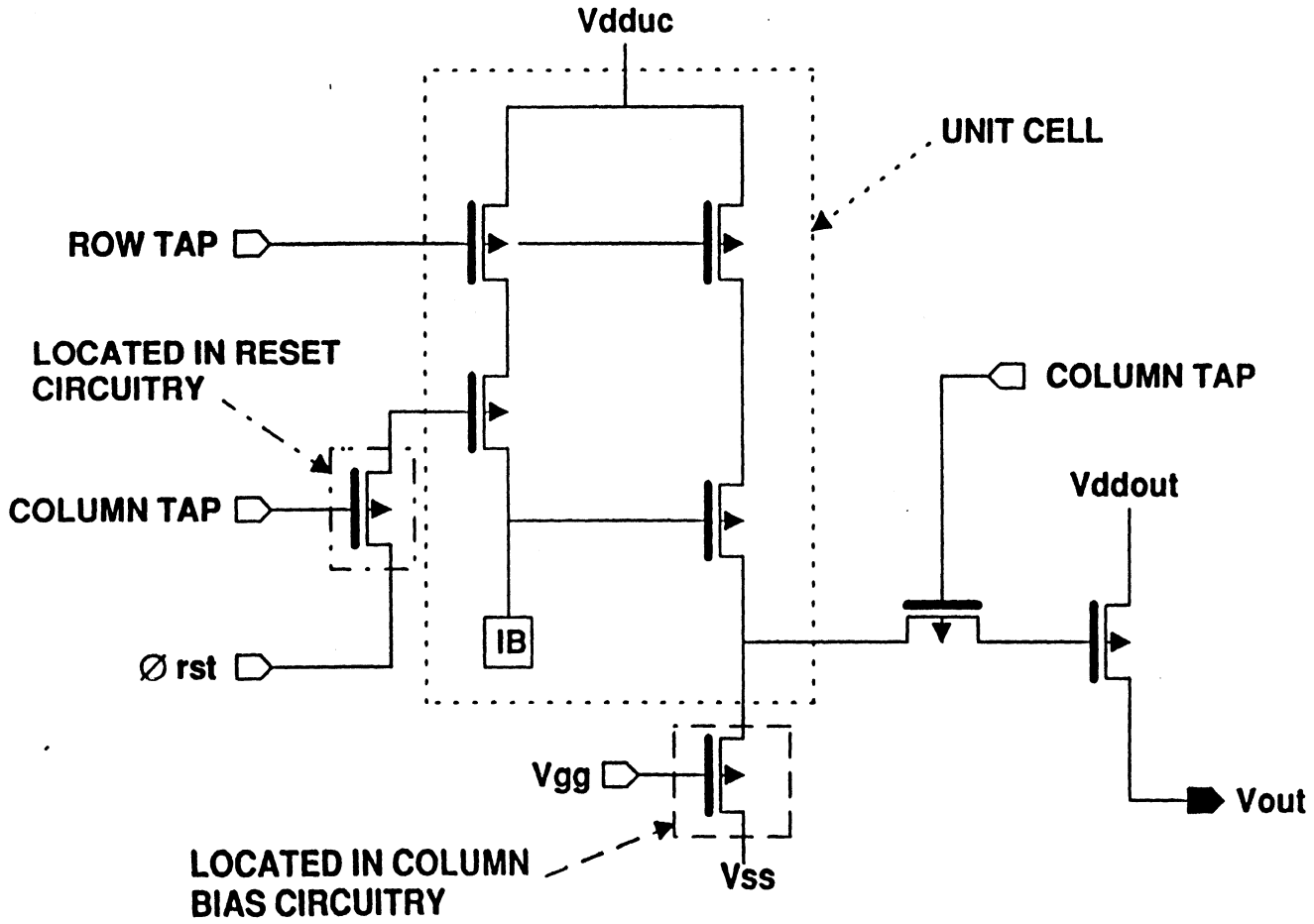
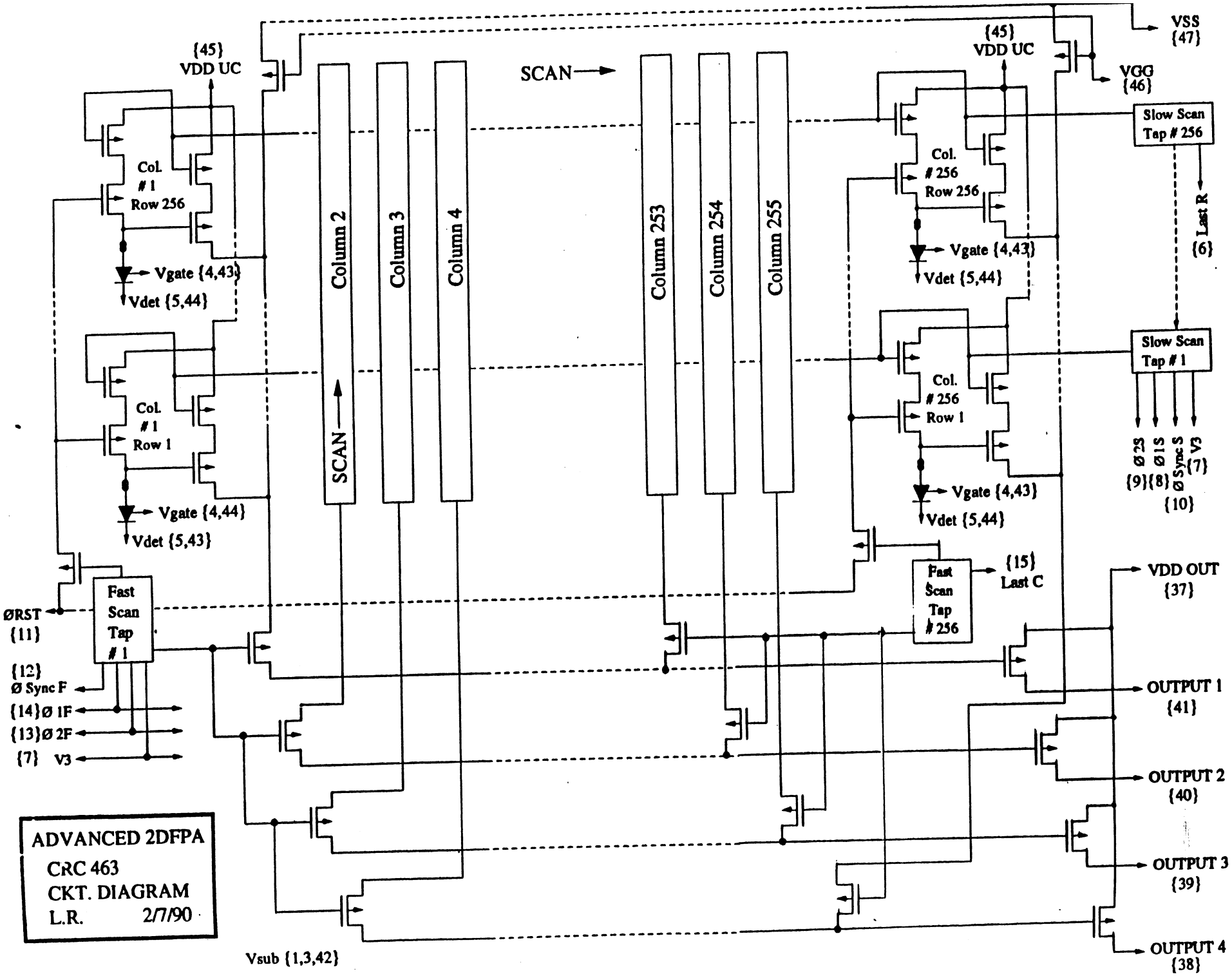
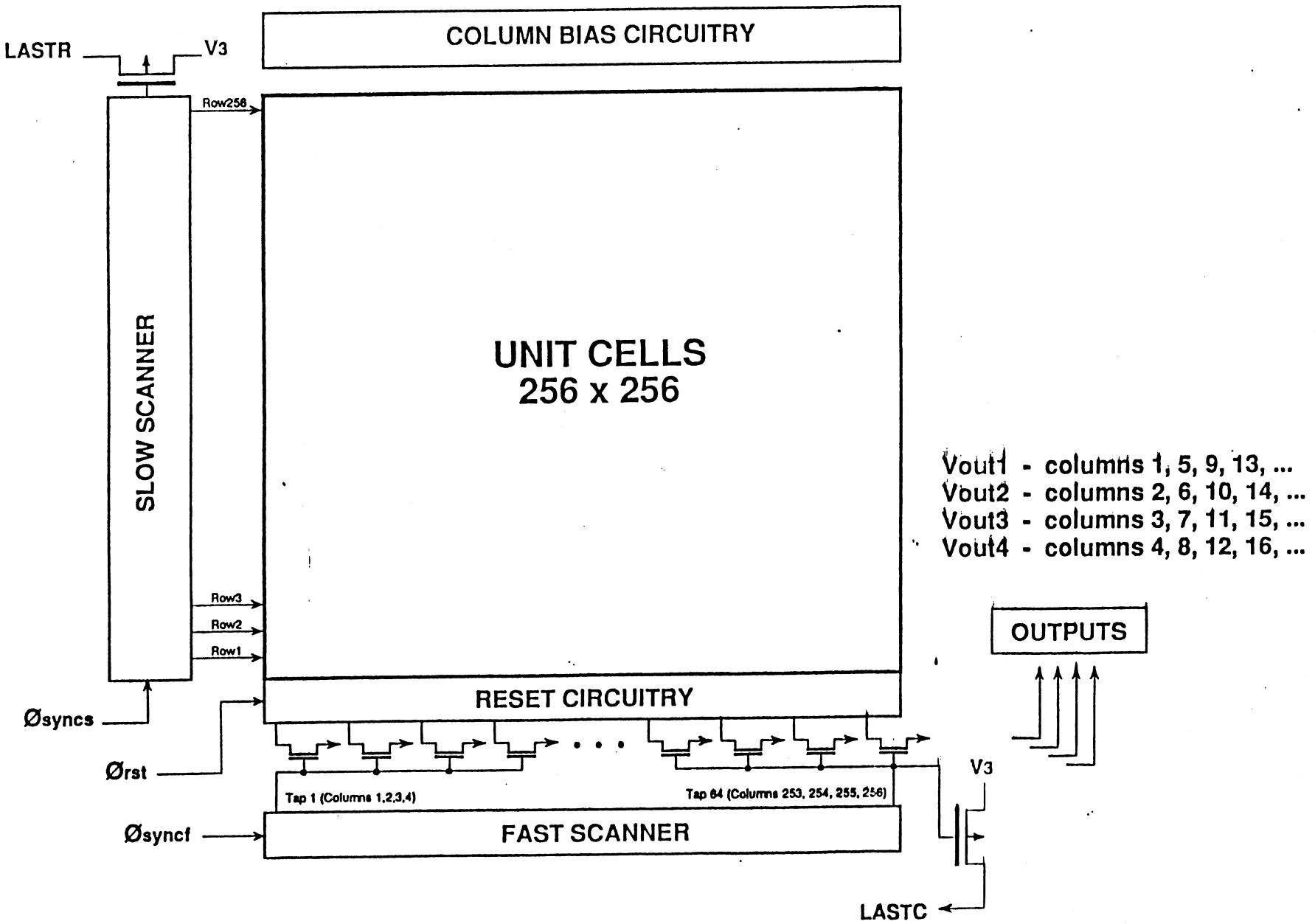


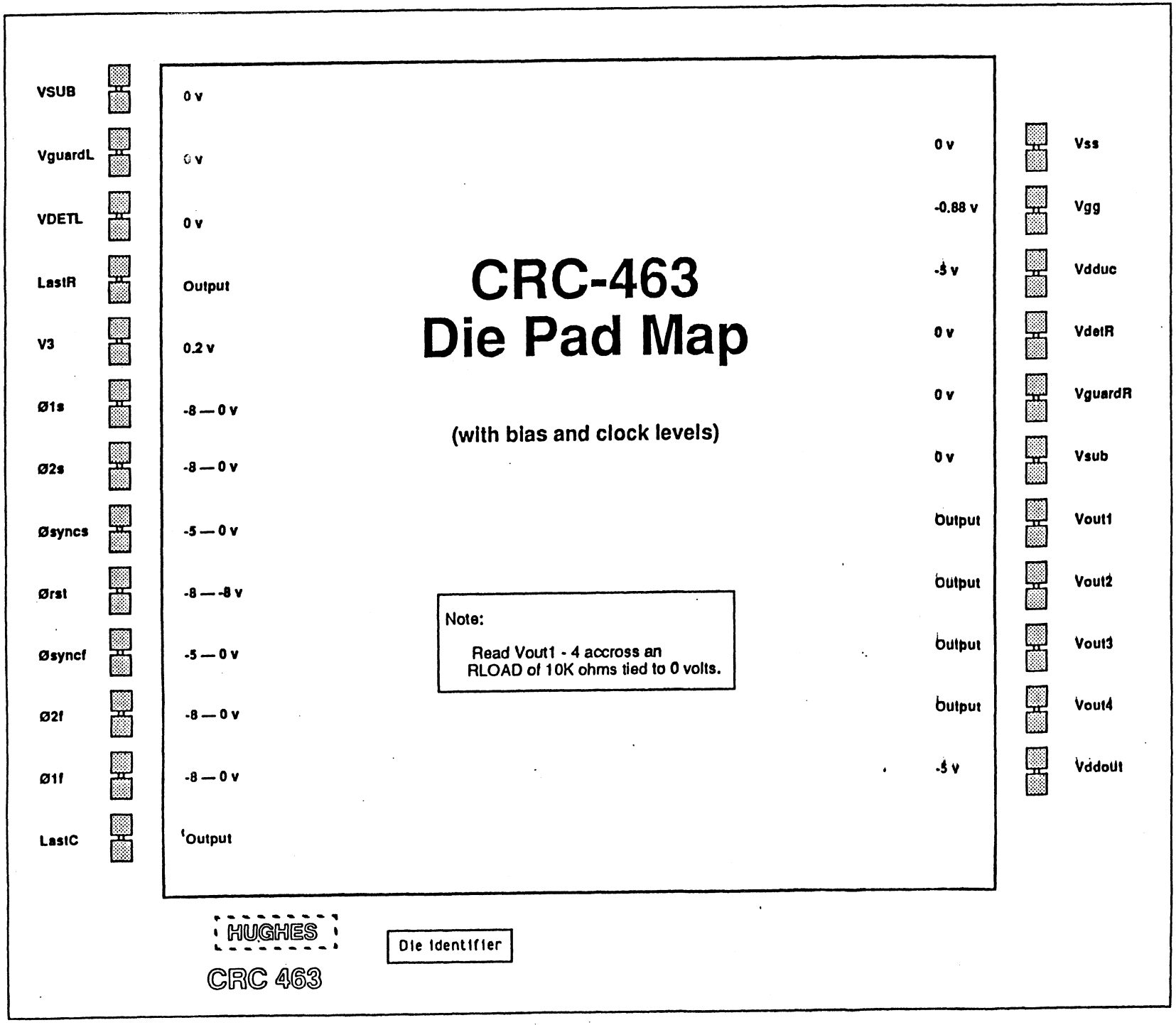
FIGURE 4

12/20/00


{45}
VDD UC
SCAN
VSS
{47}
VGG
{46}
Col.
1
Row 256
Vgate {4,43}
Vdet {5,44}
Column 2
Column 3
Column 4
Column 253
Column 254
Column 255
Col.
256
Row 256
Slow Scan
Tap # 256
Last R
{6}
Col.
1
Row 1
Vgate {4,44}
Vdet {5,43}
Col.
256
Row 1
Slow Scan
Tap # 1
Ø2S
Ø1S
Ø Sync S
V3
{9}{8}
{7}
{10}
ØRST
{11}
Fast
Scan
Tap
1
Fast
Scan
Tap
256
{15}
Last C
VDD OUT
{37}
{12}
Ø Sync F
{14}Ø 1F
{13}Ø 2F
{7} V3
OUTPUT 1
{41}
OUTPUT 2
{40}
OUTPUT 3
{39}
OUTPUT 4
{38}
Vsub {1,3,42}
ADVANCED 2DFPA
CRC 463
CKT. DIAGRAM
L.R. 2/7/90

CRC-463 PHYSICAL LAYOUT




VSUB
0 v
VguardL
0 v
VDETL
0 v
LastR
Output
V3
0.2 v
Ø1s
-8 — 0 v
Ø2s
-8 — 0 v
Øsyncs
-5 — 0 v
Ørst
-8 — -8 v
Øsyncf
-5 — 0 v
Ø2f
-8 — 0 v
Ø1f
-8 — 0 v
LastC
Output
CRC-463
Die Pad Map
(with bias and clock levels)
Note:
Read Vout1 - 4 accross an
RLOAD of 10K ohms tied to 0 volts.
0 v
-0.88 v
-5 v
0 v
0 v
0 v
Output
Output
Output
Output
-5 v
Vss
Vgg
Vdduc
VdetR
VguardR
Vsub
Vout1
Vout2
Vout3
Vout4
VddoUt
HUGHES
CRC 463
Die Identifier

CRC 463 2DFPA

SBRC Roic & Hybrid Bonding

L. Ruzicka
1/22/90
Revised
3/26/90

Scale = 5:1
Chip Carrier = 0.955" sq.
Chip = Approx. 0.372" sq.

Special Note: Bond to lower part of bond pad as drawn

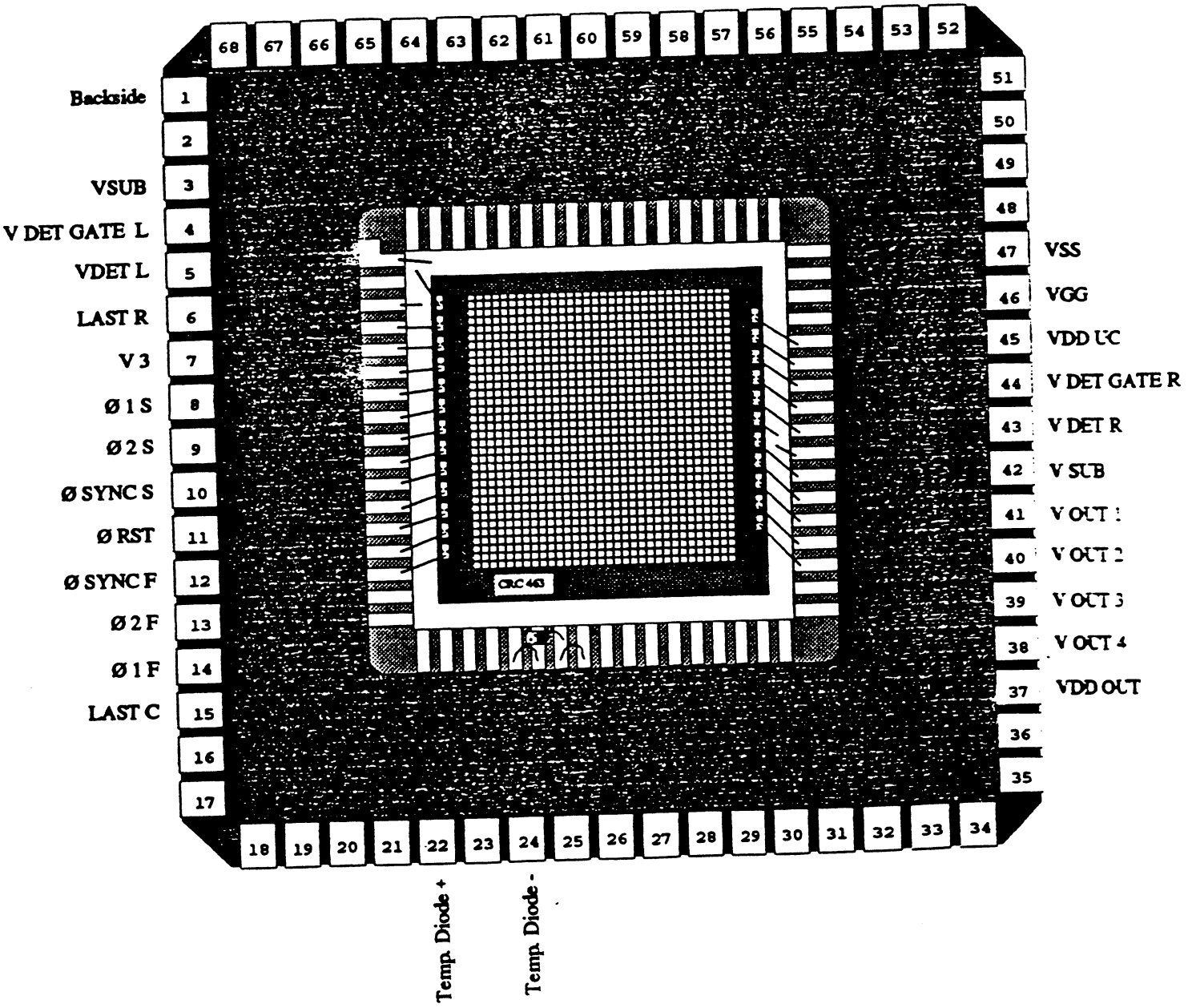


FIGURE 2

12/20/90

SANTA BARBARA RESEARCH CENTER

A Subsidiary of Hughes Aircraft Company

MEMORANDUM

TO: Bill Forest
University of Rochester
Dept of Physics and Astronomy

DATE: 2/9/91

REF:

FROM: Lee Ruzicka

SUBJECT: Follow up to our Feb. 4th conversation

BLDG: B1 MAIL STA. 51
Ph. No.: (805) 562-2783

As promised, this memo is being forwarded to you by standard ground mail as added clarification to the FAX'ed memo sent to you earlier. The forward part of this memo is identical to the FAX'ed memo, the ladder part, with actual photo's, has been added as an enhancement.

In our conversation on Feb. 4th you had asked a number of questions regarding the operation of the CRC 463 FPA. I've listed your questions and my answers. If more clarification is needed, don't hesitate to give me a call at the phone number listed above. Please note that this particular memo was written to provide clarity to a FAX transmission, and that actual photo's depicting the CRC 463 FPA waveforms will be sent to you through standard ground mail as soon as possible.

1. What method does SBRC use to measure internal device gain?

Our method of measuring the internal gain of the CRC 463 InSb FPA is as follows: The detector substrate, and the detector gate are tied to VDD UC. All other clock and biases remain at their nominal voltages. VDD UC is then adjusted to the low end of the dynamic range ≈ -2.9 volts, whereupon the output DC level is sampled. Next VDD UC is adjusted to near the high end of the dynamic range, ≈ -3.5 volts, and the output DC level is once again sampled. Δ Vout / Δ Vin is applied to obtain the internal gain of the FPA. Detector substrate, and the detector gate are tied to VDD UC to insure the protection of the detector diode by keeping the potential across the detector constant, this also removes any ambiguities that could be introduced by variations detector impedances. This method is used at warm and cold temperatures with small variations in gain, (≈.6 to .7) due to threshold shifts between warm and cold temperatures.

2. What is the output DC level

With the output source followers biased with a 10K resistor to ground the output DC level should have a nominal voltage of ≈ - 300mv at the reset period. This is affected by the VDD UC and VDET voltages.

3. We need a depiction of what pixel output waveform to expect

Figure 1 describes a three pixel waveform set at room temperature. In order to eliminate high electric field conditions across the detector gate, and possible damage to the detector gate, Vgate and Vdet are connected to VDD UC under room temperature conditions. Therefore the output waveform at room temperature will appear quite uniform with pixel to pixel variations of ≈ 10 to 20mv except where open or leaky detectors are present.

Figure 2 describes a three pixel waveform set at cryogenic temperatures. Pixel "A" is what to expect when Vgate ≈ Vdet, where a condition we term "Charge dumping" is actually de-biasing the detector. Pixel "B" depicts a well biased detector in the dark with idealized dark current. Pixel "C" is the same as "B" except the detector is now being irradiated with light.

Figure 1

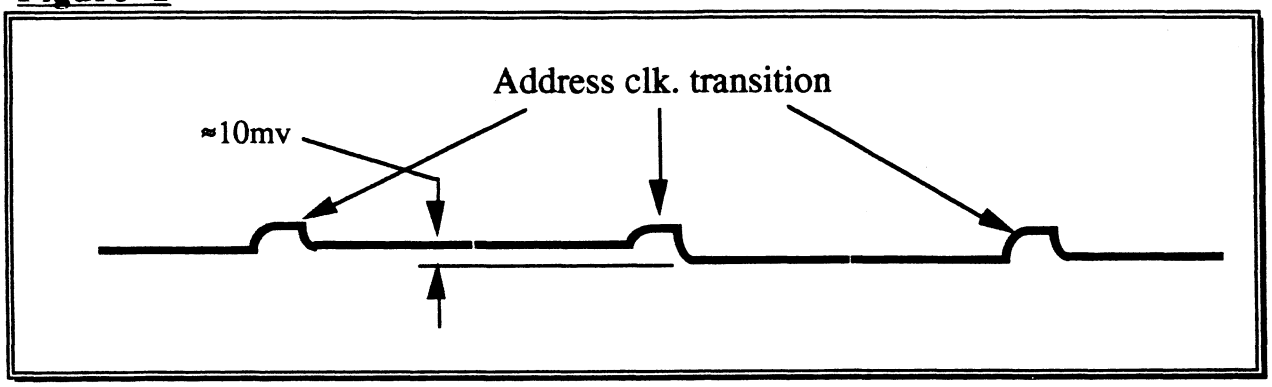
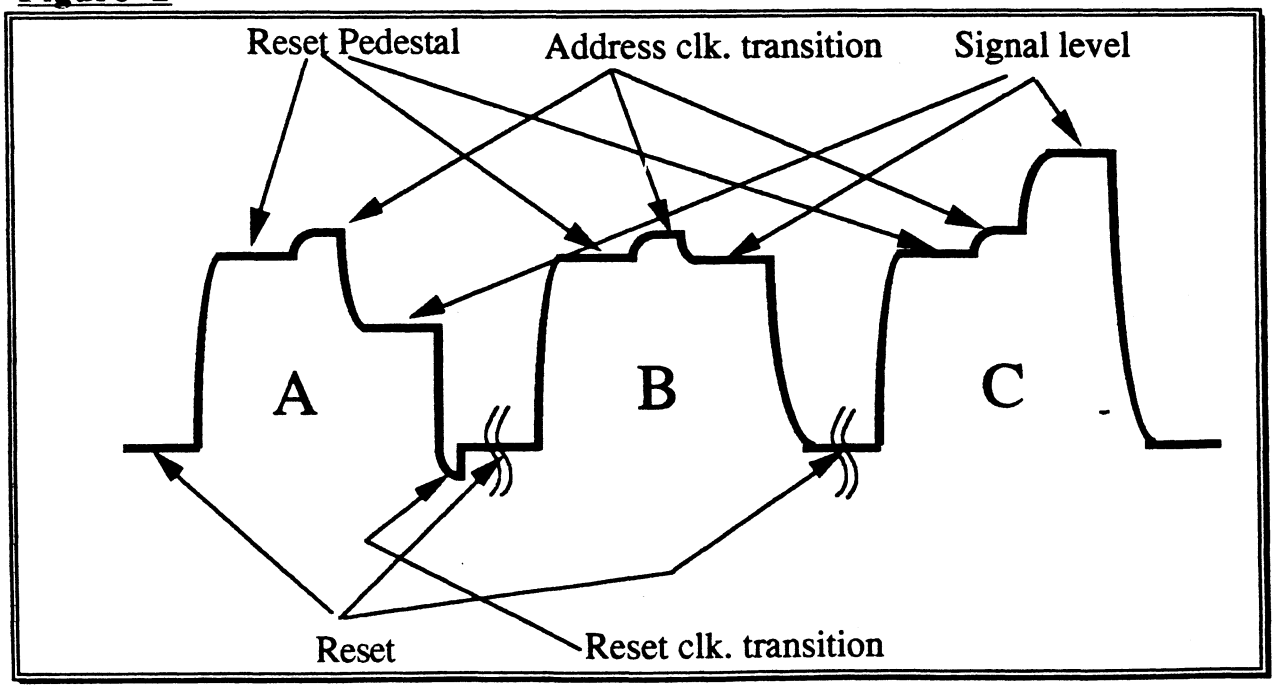


Figure 2



4. Describe the LAST C and the LAST R output waveforms.

Basically the LAST C and the LAST R outputs were intended to indicate if the array scanner were functioning or not. In actual testing it was found that these indicators were not reliable; i.e. on some arrays these outputs failed while the actual array functioned perfectly, and conversely the LAST C and the LAST R functioned but the actual array did not. Photo's of these outputs will be sent to you with the ground mailing of this memo. The LAST C should have a one pixel wide pulse that occurs at the same time as the last column in each row that is read out. The LAST R should have a one row wide pulse that occurs at the same time as the last row in every frame. Both outputs should be negative going in nature, and be ≈ 1 volt in amplitude. The LAST C and the LAST R outputs need to be loaded with a 10K ohm resistor.

5. Does a temperature diode curve for the 1N914 temperature diode exist.

A temperature vs diode voltage curve and tabulation is attached.

Lee Ruzicka

LEE RUZICKA - TEST REA
TEST AND EVALUATION SECTION

APPROVED:

TOM KOCH - SECTION HEAD
TEST AND EVALUATION SECTION

APPROVED:

RON MASCETELLI- LAB MGR.
TEST AND EVALUATION SECTION

CRC 463 OUTPUT WAVEFORM PHOTOS

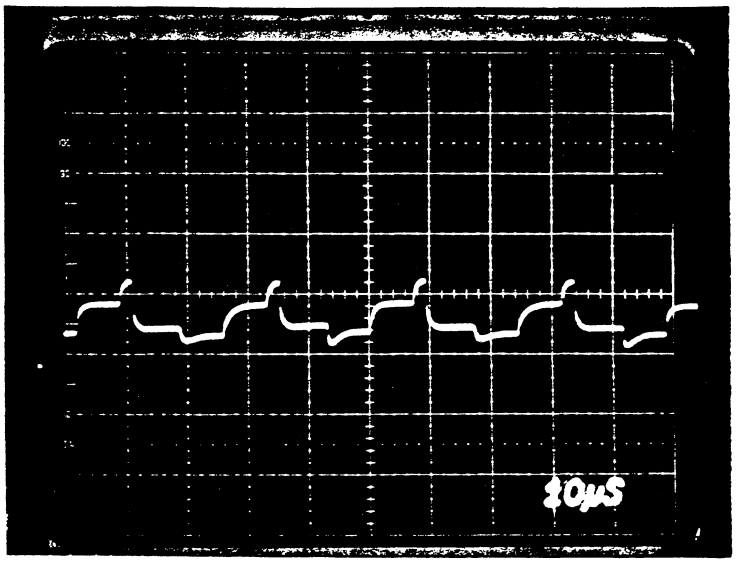


PHOTO NO. 1
Four complete pixels showing

50mv / Div.
Vdet = zero bias
Vgate = -3.0 volts
Temperature = 50K

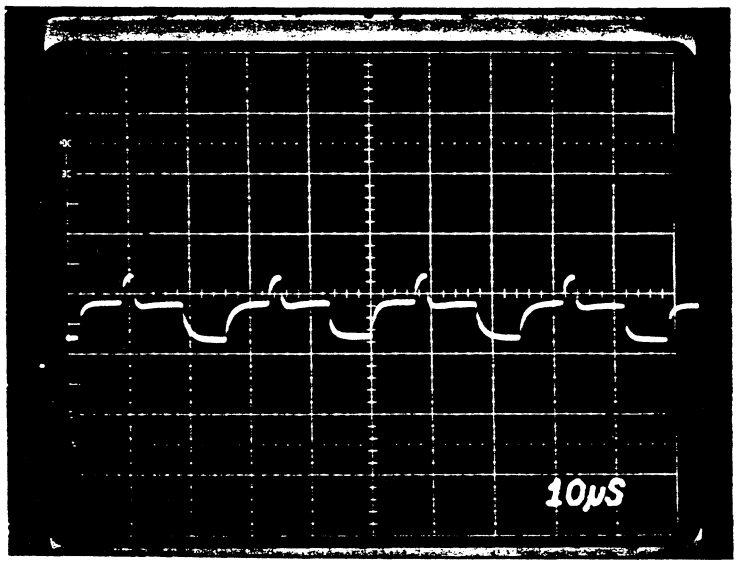


PHOTO NO. 2
Four complete pixels showing

50mv / Div.
Vdet = 300mv
Vgate = -4.5 volts
Temperature = 50K

NOTE: Refer to accompanying memo for an anatomy of the above waveforms

CRC 463 OUTPUT WAVEFORM PHOTOS

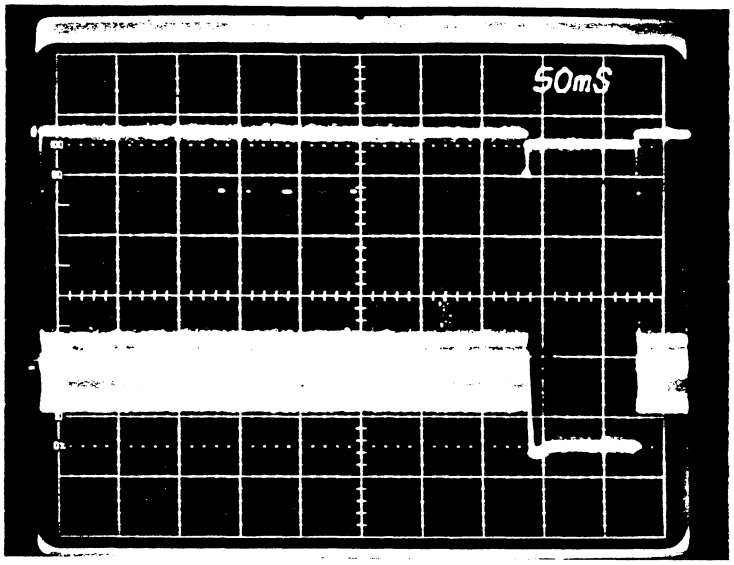


PHOTO NO. 3

LAST R OUTPUT
Overview photo at end of frame
2 volts / Div.

DEVICE OUTPUT
50mv / Div.

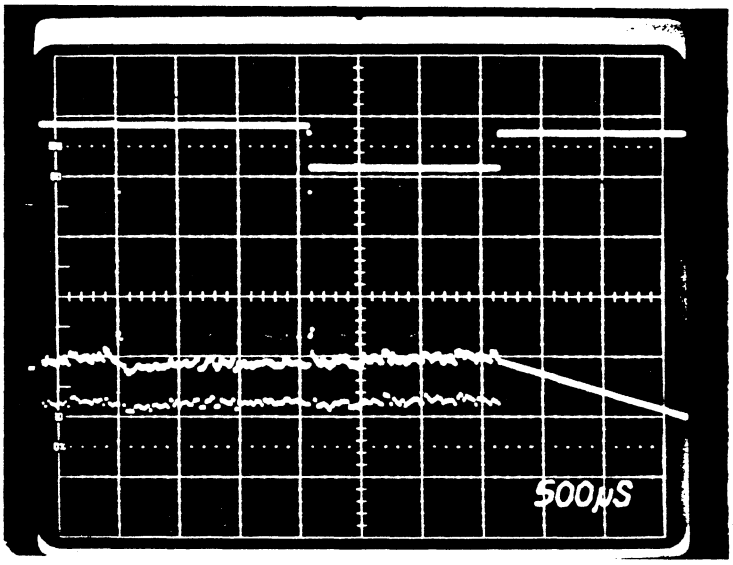


PHOTO NO. 4

LAST R OUTPUT
Expanded photo at end of frame
2 complete rows showing
2 volts / Div.

DEVICE OUTPUT
50mv / Div.

NOTE: In both photo's, a single open detector defect is present at the end every row, (positive going pulse) and could be confused with the LAST R output because of it's close proximity to the LAST R output.

The ≈ 10mv neg. going step at the end of the frame in the LAST R output, is due to a non-clocked period used to control the integration time. A similar but larger step is also seen in the device output.

CRC 463 OUTPUT WAVEFORM PHOTOS

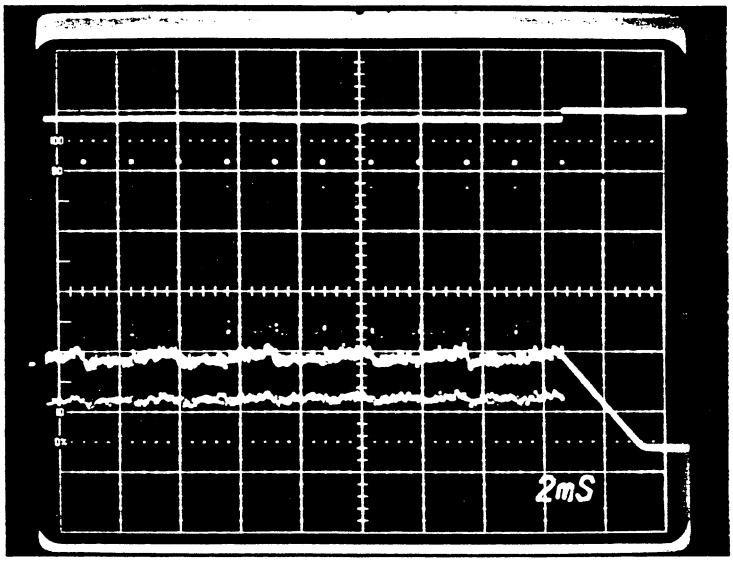


PHOTO NO. 4

LAST C OUTPUT
Overview photo at end of frame
2 volts / Div.

DEVICE OUTPUT
50mv / Div.

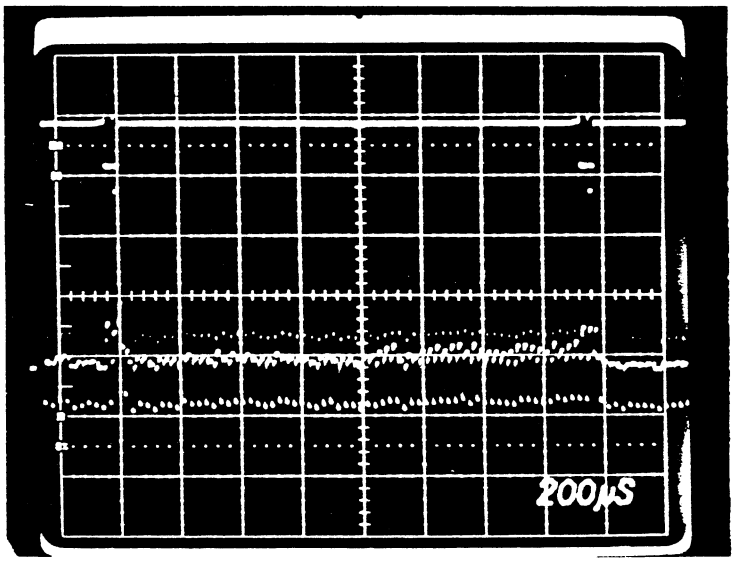


PHOTO NO. 5

LAST C OUTPUT
Expanded photo at end of frame
1 complete row showing
2 volts / Div.

DEVICE OUTPUT
50mv / Div.

NOTE: As in photo's 3 & 4, a single open detector defect is present at the end every row, (positive going pulse) and could be confused with the LAST R output because of it's close proximity to the LAST R output.

In close examination of the LAST R output pulse, it noted that a second pulse is present and is in coincidence with the open detector described earlier. This anomaly has not been observed in previous devices. An explanation for this phenomena would be only speculative at this time.