IRLabs, Inc.

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Tucson, AZ 85719 - 6505 / USA
Phone # : 520 - 622 - 7074
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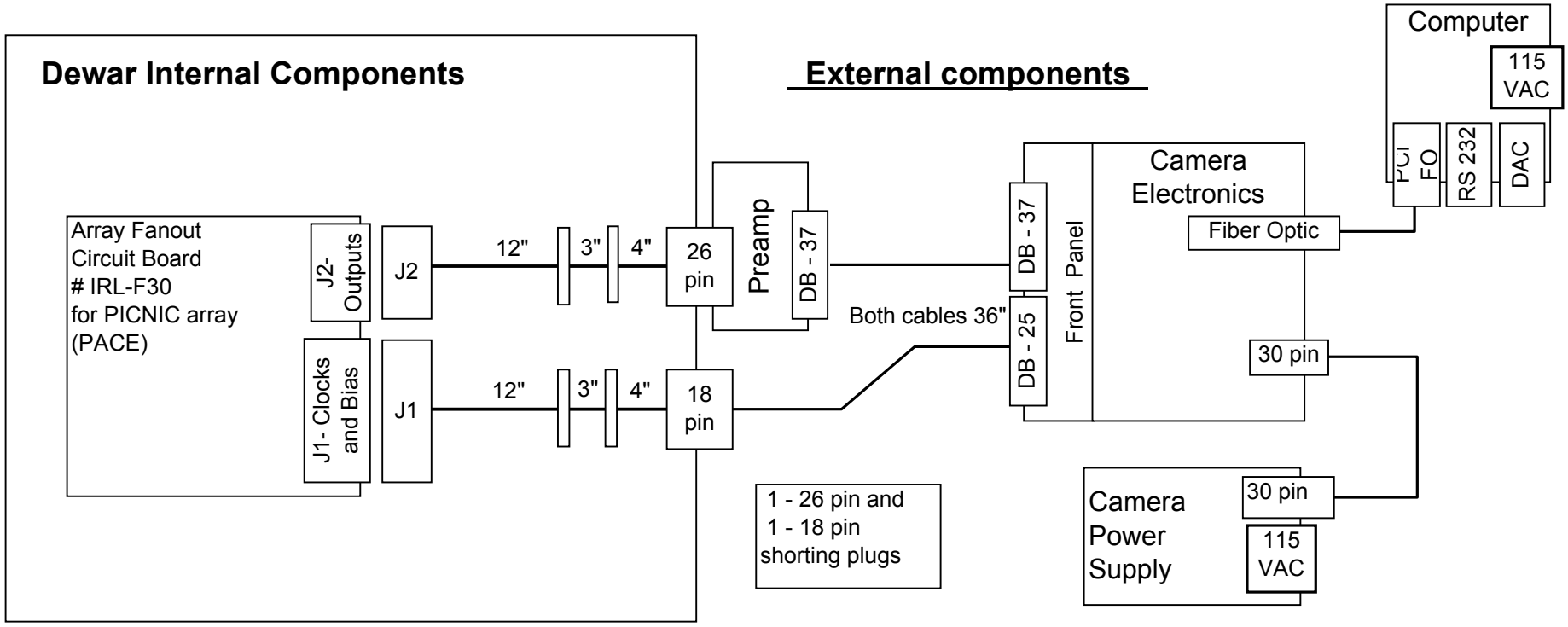
Customer :	University of Michigan
P.O. number :	UMCHND03Z
Dewar number :	3625
Job Order number :	1331
Quote number :	
Components :	IRLF30 - PICNIC (PACE) Array Components, Motor Drive will be added later.

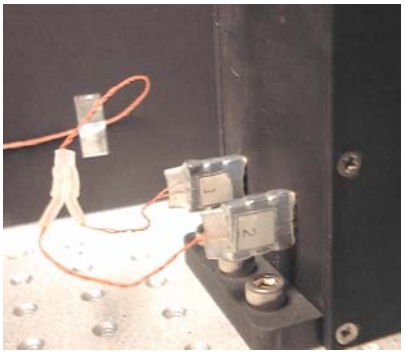
Array Components Parts List :

	IRL F30 Circuit Board
	Internal Analog Cable
	Internal Digital Cable
	External Analog Cable
	External Digital Cable
	IREMB Preamp
	18 and 26 pin, Shorting Plugs


Dewar Internal Components
External components
Array Fanout
Circuit Board
IRL-F30
for PICNIC array
(PACE)
J2- Outputs
J2
J1- Clocks and Bias
J1
12"
3"
4"
12"
3"
4"
26 pin
18 pin
Preamp
DB - 37
Both cables 36"
DB - 37
DB - 25
Front Panel
Camera Electronics
Fiber Optic
30 pin
Computer
115 VAC
PCI FO
RS 232
DAC
1 - 26 pin and
1 - 18 pin
shorting plugs
Camera Power Supply
30 pin
115 VAC

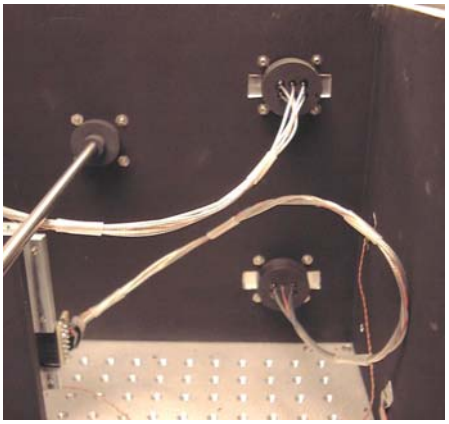
Inside Dewar Layout

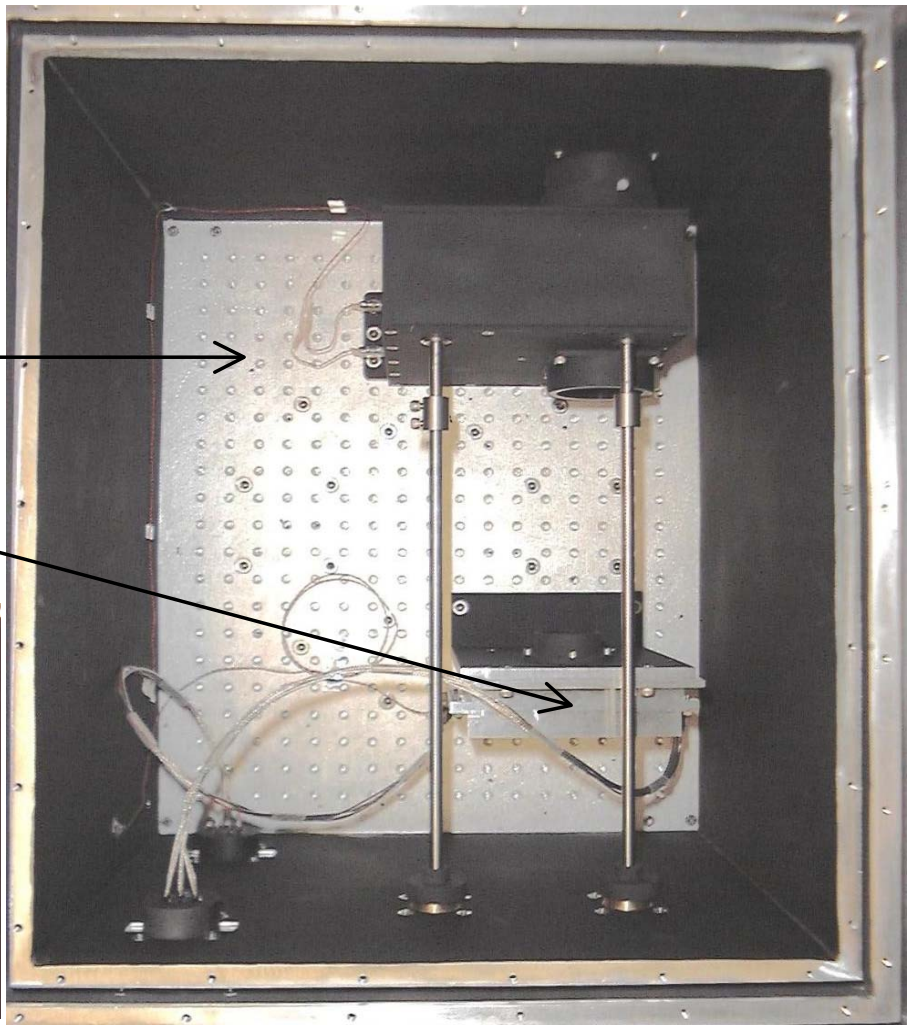
Filter Wheel Box connectors



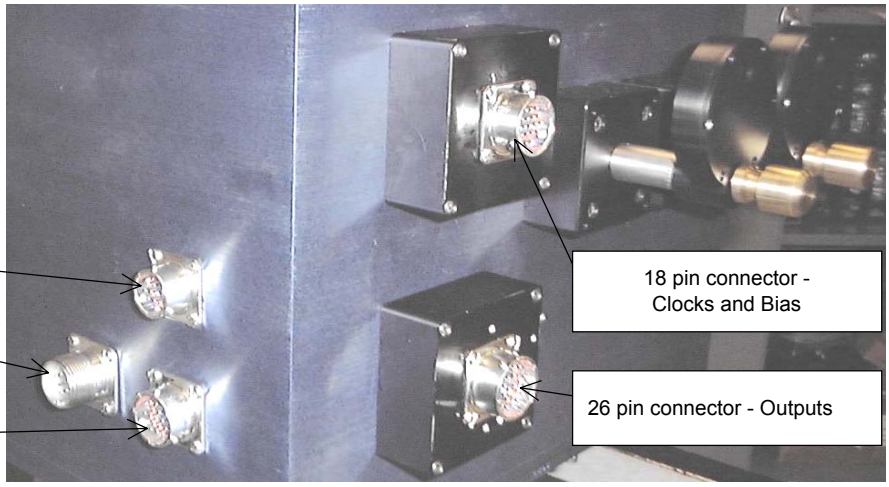
Array mount

Array Cable Heatsinks



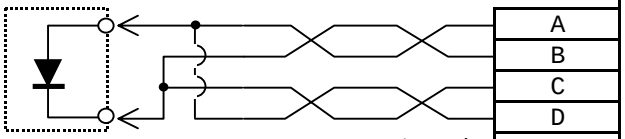


Dewar case connectors



Dewar Internal wiring

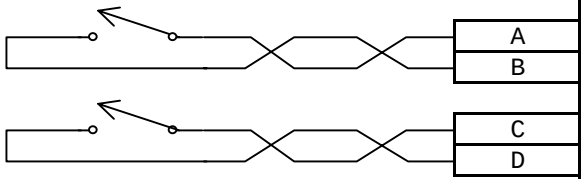
10 pin
Hermetic connector



	A	I +
	B	I -
	C	V -
	D	V +
not used	E	
not used	F	
not used	G	
not used	H	
not used	J	
not used	K	

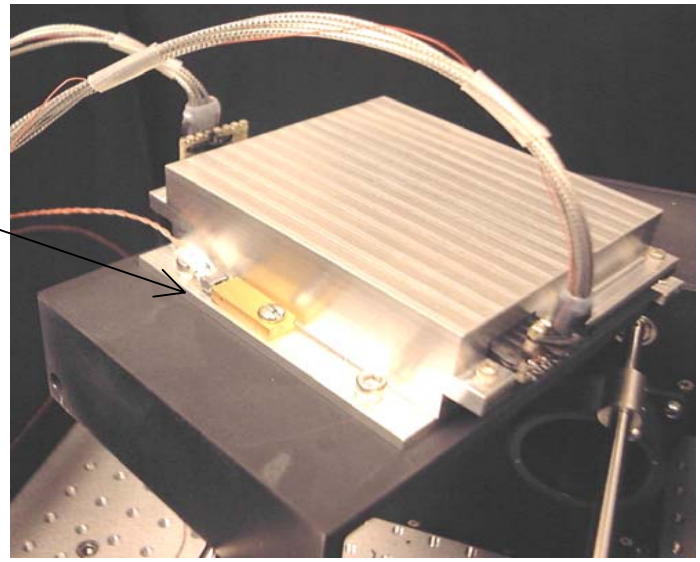
Filter Wheel Box Home Switches
Open at Home Position

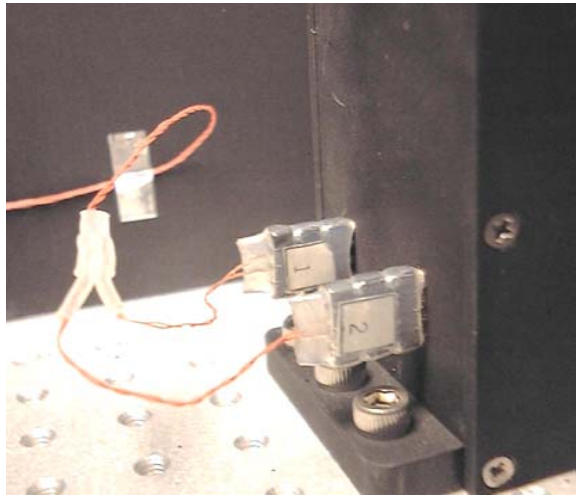
6 pin
Hermetic connector



# 1	A	
	B	
# 2	C	
	D	
not used	E	
not used	F	

Temperature Sensor on
Array Mount





1 is near the
Dewar window

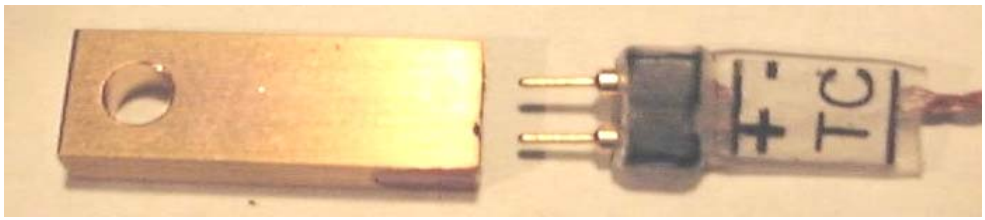
Temperature Sensor connections

MMSD - Moveable Mount Silicon Diode

this side should face up

mount this side toward cold work surface

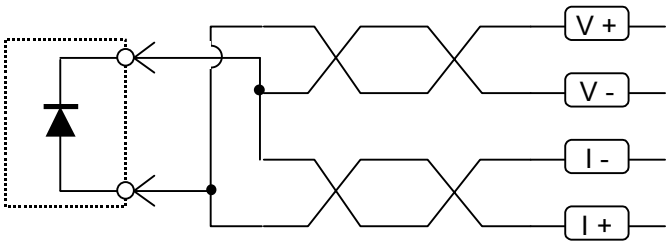
polarity marks on sensor and cable connector indicate the positive side



mount hole red mark

On the sensor connector "TC" indicates Temperature Control cable. The "TC" cable is intended to be used to control nearby heater elements. A number indicates the readout sensors position on the Dewars case connector.

Wiring diagram of sensor and twisted pair cable inside Dewar



use an ohm meter to check polarity of final wiring. (similar to a diode)
at room temperature : forward bias is around 3.5 MΩ
reverse bias is infinite.
at nitrogen temperature : forward bias is around 18 MΩ
reverse bias is infinite.

JC#, DWR # : UMCHND03Z - 3625 2/24/04
board use notes : PICNIC Board configured for PACE
circuit board # : IRLF 30
circuit board S/N # : 009

	TEST DATES	assembler initials	testers initials
general appearance			
circuit board cleaned, no finger prints, flux residue, dross, etc..			
all connectors and components parallel or vertical to board			
all solder joints filled, no voids, orange peel or cold solder joints			
fiberglass, thermal layers and pads not damaged			
FPA socket installed correctly			
pin #1 is over board pin #1 marking			
socket feet touch the thermal layer			
corners bottom edges are same distance from the thermal layer			
contact pins are not bent in or dirty			
all TANTALUM capacitors			
7 caps installed - C2 through C5 not installed all others are 16V/10μF			
bottom touches the board			
polarity correct			
no shorts to thermal layer			
other			
all 5 jumpers are installed			
Jumper configuration for PACE : J6 pins 1 to 2, J7 pins 2 to 3			
key pins are clipped : J1 pin 10, J2 pin 8			
serial number is scratched on the back upper left side (J1 and J2 at bottom)			
SIP / Rpack resistors oriented correctly			
SIP / Rpack resistors are ceramic type			
top and back pictures are in focus and copied to the bottom of data sheet)			
JFETS			
bottom edge of the JFET .060" away from board (20 AWG wire thickness)			
no shorts from any of the 3 pins to the thermal layers			
installed correctly (orientation of drain, source and gate to board)			
cold test - data sheet is filled in completely			

Individual JFET - Source Voltage Test

Drain Voltage = 5.0 V
JFET Gates = Ground
match range = .001 V
source resistor used for test = 19.97 K

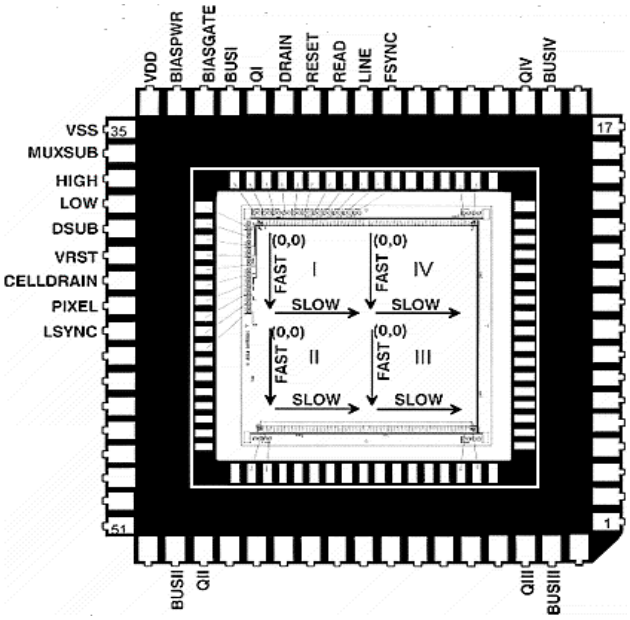
JFET Serial #	VS ~300 K	VS ~77 K
496	1.000	0.669
426	0.965	0.669
613	0.987	0.670
730	0.988	0.670

Assembled Board Final JFET - Source Voltage Test

JFET Gates = Grounded through blank LCC chip
Drain Voltage = 5.04 V
match range = 0.002 mV
installed RS value at 77K = 20.1 K Ω

Installed Position	JFET Serial #	VS ~300 K	VS ~77 K
Q1	496	1.006	0.673
Q2	426	0.973	0.672
Q3	613	0.995	0.673
Q4	730	0.996	0.674

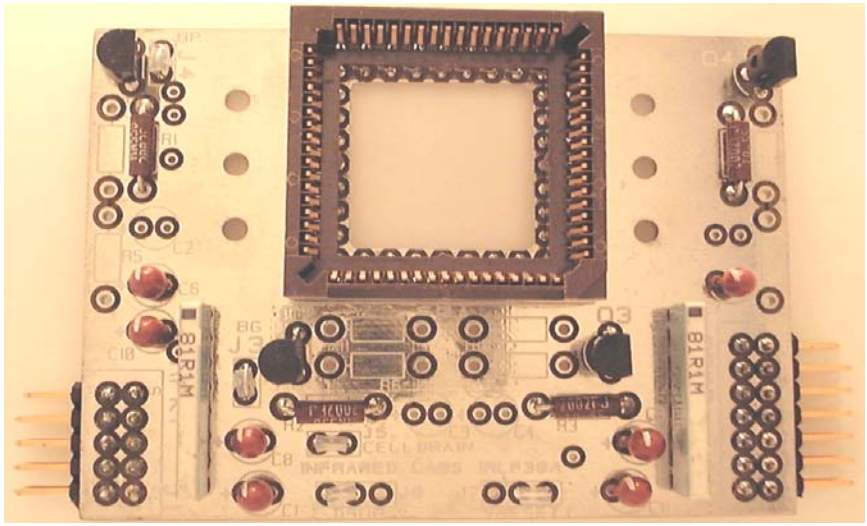
JC#, DWR # : UMCHND03Z - 3625
board use notes : PICNIC Board configured for PACE
circuit board # : IRLF 30
circuit board S/N # : 009



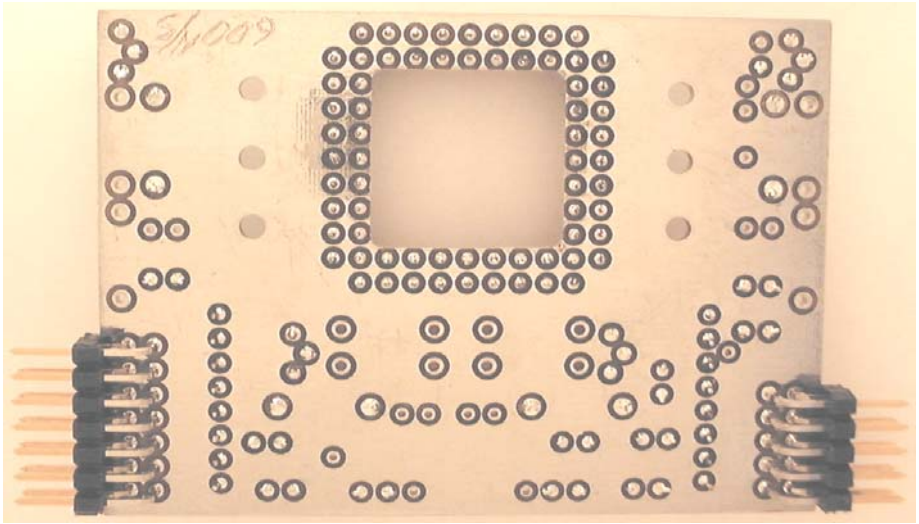
Jumper
Configurations :
MBE :
J6 = 2 - 3
J7 = 1 - 2

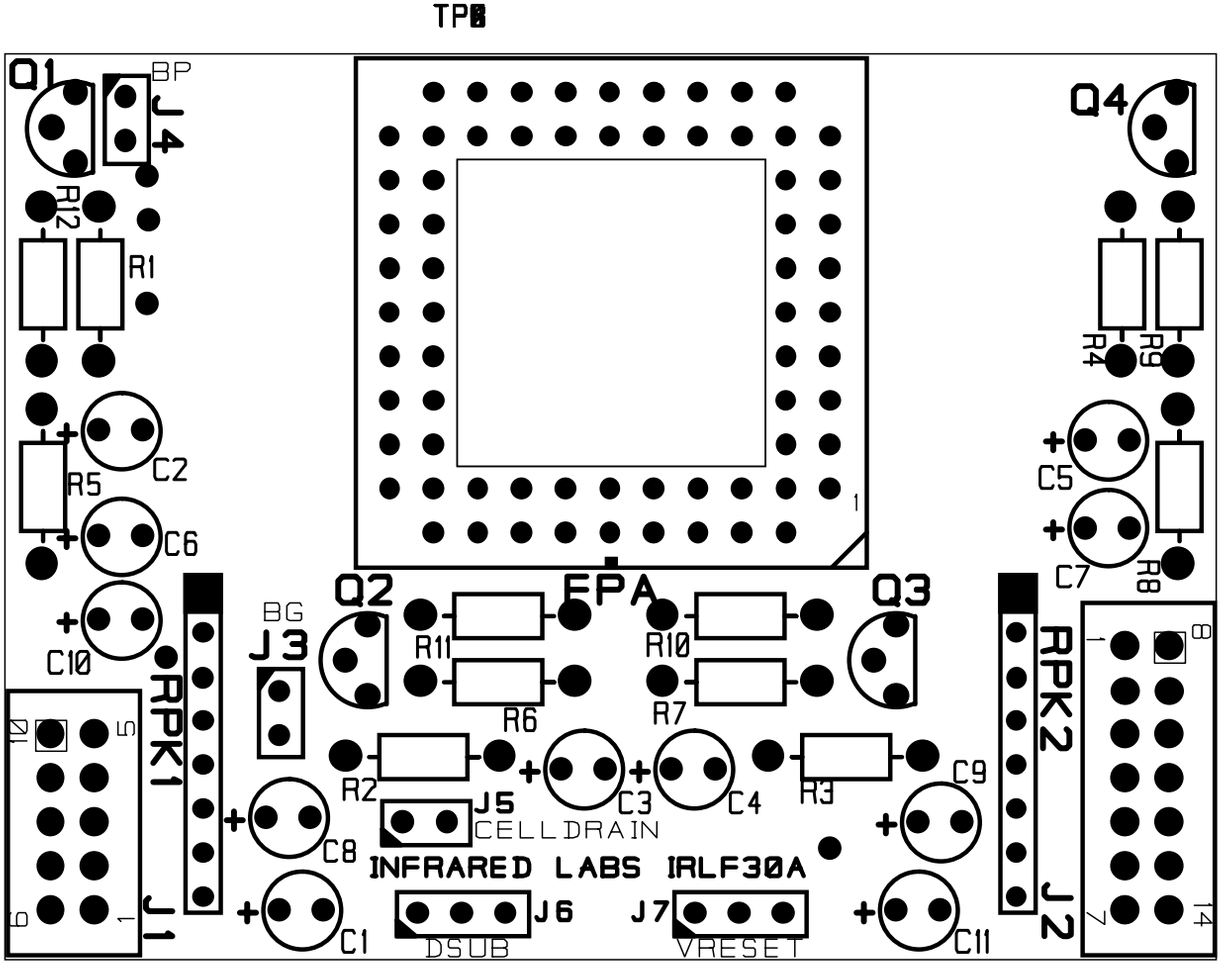
PACE :
J6 = 1 - 2
J7 = 2 - 3

TOP VIEW

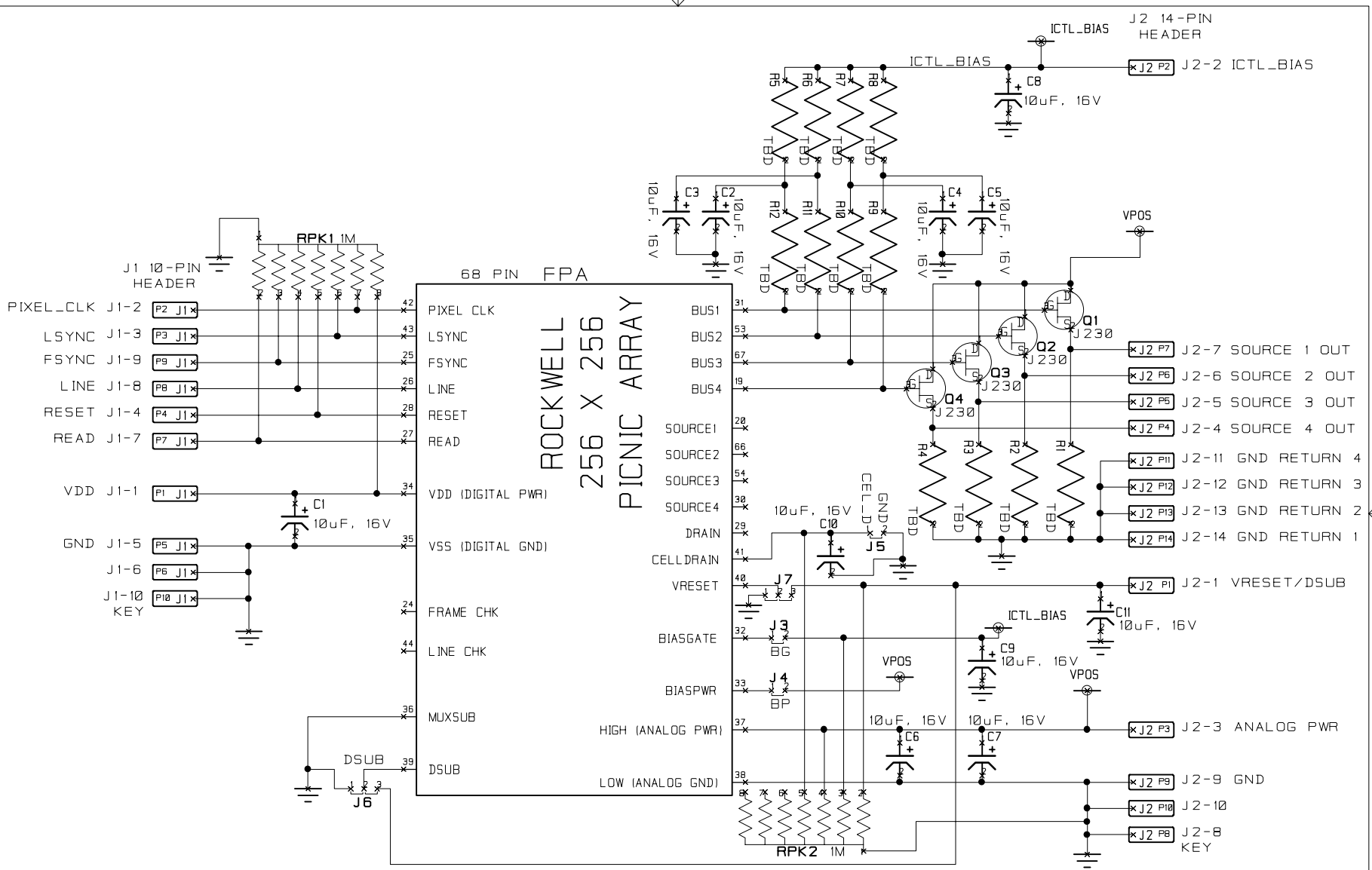


BACK VIEW





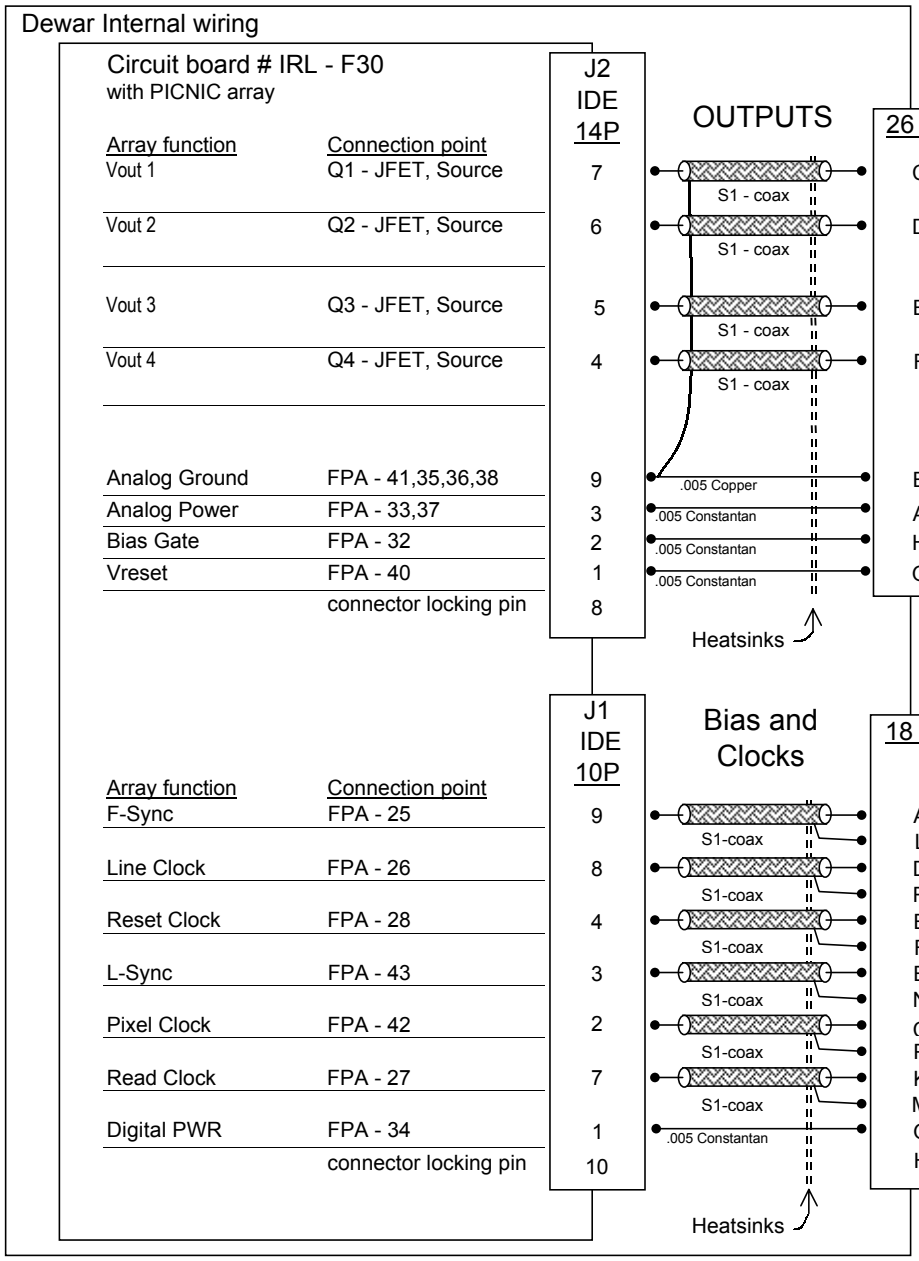
L1 SILKSCREEN



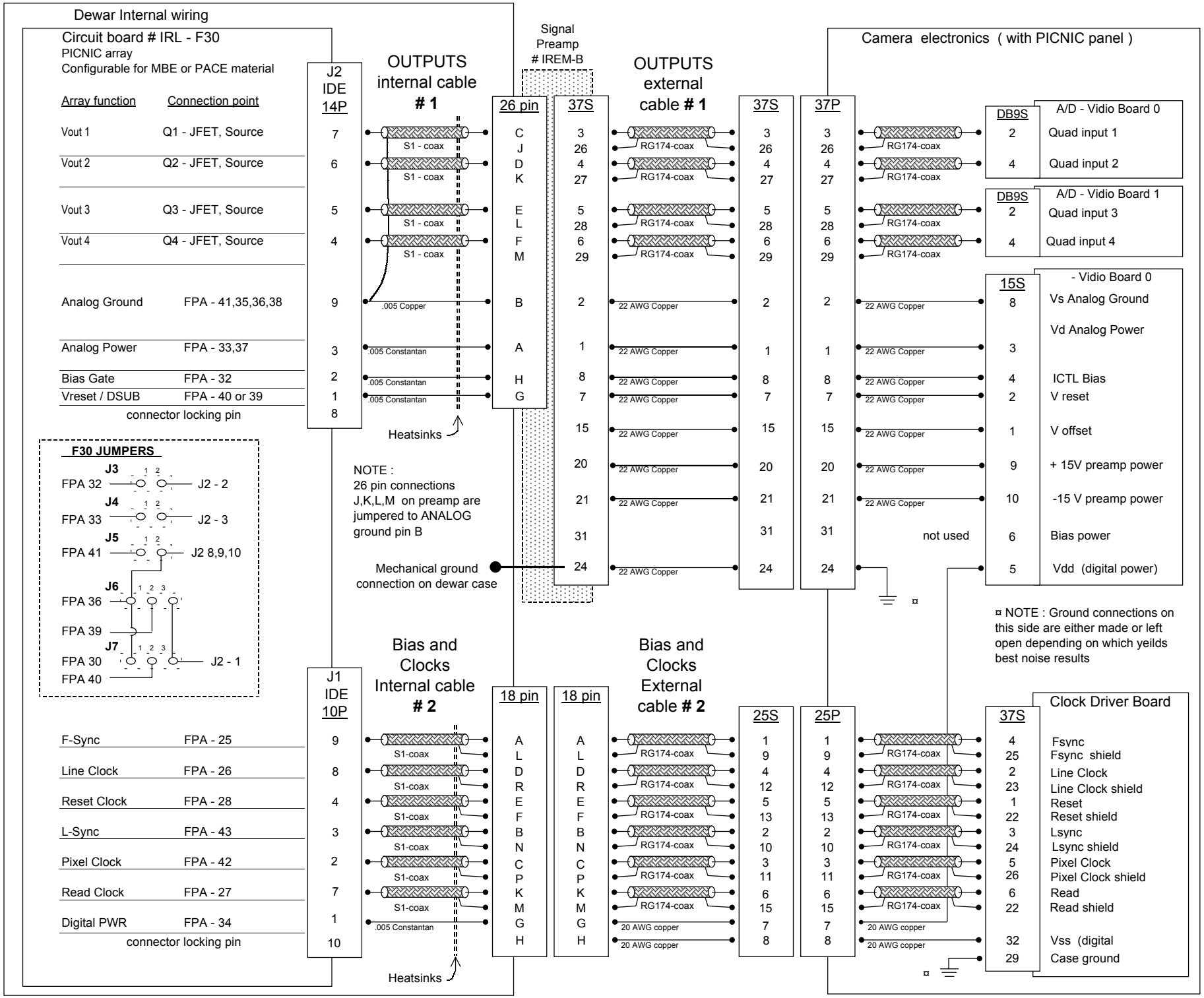
MOUNTING HOLES

TP1 TP2 TP3 TP4 TP5 TP6

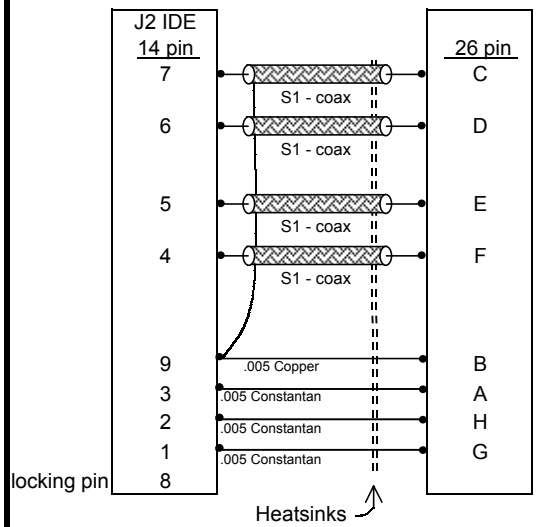
CONTRACT NO. RDMIC		COMPANY NAME INFRARED LABORATORIES, INC.	
APPROVALS	DATE	DWG IRLF30A PICNIC FANOUT BOARD vs.2	
DRAWN	2/16/2000	SIZE A	FSCM NO. / DWG NO. / REV. A
CHECKED			
ISSUED		SCALE	PAUL ARBO / SHEET 1 OF 1



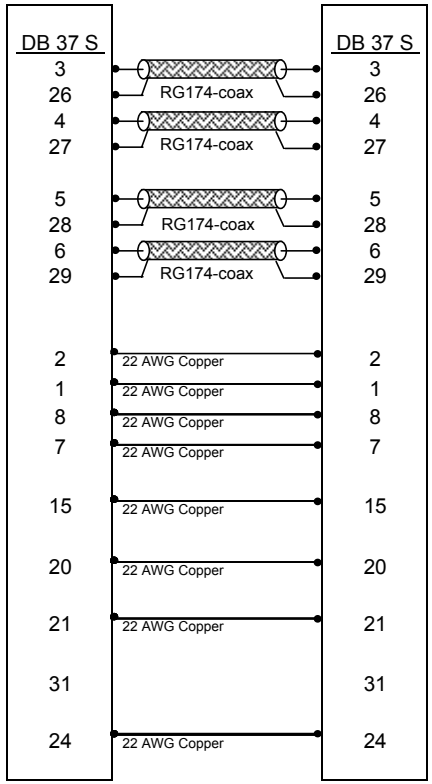
	Test Date 1/23/04 Wire resistance end to end test at **300 K**	Test Date 1/27/04 Shorting chip Continuety test at **300 K**	Test Date 2/5/04 Shorting chip Continuety test at **77 K**
Vout 1	10.3 Ω	502 Ω	307.7 Ω
Vout 2	10.2 Ω	674 Ω	304.2 Ω
Vout 3	10.2 Ω	670 Ω	483 Ω
Vout 4	10.2 Ω	671 Ω	470 Ω
Analog Ground	1 Ω	Ground / Reference Ω	Ground / Reference Ω
Analog Power	23.3 Ω	24.2 Ω	36.6 Ω
Bias Gate	23.2 Ω	24.4 Ω	36.5 Ω
Vreset	23.3 Ω	24.5 Ω	36.6 Ω
F-Sync	10.2 Ω	11.2 Ω	8.5 Ω
S1-coax	∝	∝	∝
Line Clock	10.2 Ω	11.2 Ω	8.5 Ω
S1-coax	∝	∝	∝
Reset Clock	10.3 Ω	11.1 Ω	8.5 Ω
S1-coax	∝	∝	∝
L-Sync	10.3 Ω	11.1 Ω	8.5 Ω
S1-coax	∝	∝	∝
Pixel Clock	1.0 Ω	11.1 Ω	8.5 Ω
S1-coax	∝	∝	∝
Read Clock	10.4 Ω	11.2 Ω	8.5 Ω
S1-coax	∝	∝	∝
Digital PWR	23.7 Ω	24.9 Ω	37.0 Ω
All coax center conductors should be isolated from coax shields :	infinite	infinite	infinite
All connections should be isolated from dewar case / ground, unless otherwise indicated :	infinite	infinite	infinite
TESTED BY :	MWR	MWR	MWR


Dewar Internal wiring
Circuit board # IRL - F30
PICNIC array
Configurable for MBE or PACE material
Array function
Connection point
Vout 1
Q1 - JFET, Source
Vout 2
Q2 - JFET, Source
Vout 3
Q3 - JFET, Source
Vout 4
Q4 - JFET, Source
Analog Ground
FPA - 41,35,36,38
Analog Power
FPA - 33,37
Bias Gate
FPA - 32
Vreset / DSUB
FPA - 40 or 39
connector locking pin
J2 IDE 14P
7
6
5
4
9
3
2
1
8
OUTPUTS internal cable # 1
S1 - coax
.005 Copper
.005 Constantan
Heatsinks
26 pin
C
J
D
K
E
L
F
M
B
A
H
G
Signal Preamp # IREM-B
37S
3
26
4
27
5
28
6
29
2
1
8
7
15
20
21
31
24
OUTPUTS external cable # 1
RG174-coax
22 AWG Copper
37S
37P
Camera electronics (with PICNIC panel)
DB9S
A/D - Vidio Board 0
2
Quad input 1
4
Quad input 2
A/D - Vidio Board 1
Quad input 3
Quad input 4
15S
- Vidio Board 0
8
Vs Analog Ground
Vd Analog Power
3
4
ICTL Bias
2
V reset
1
V offset
9
+ 15V preamp power
10
-15 V preamp power
6
Bias power
5
Vdd (digital power)
not used
NOTE :
26 pin connections J,K,L,M on preamp are jumpered to ANALOG ground pin B
Mechanical ground connection on dewar case
¤ NOTE : Ground connections on this side are either made or left open depending on which yeilds best noise results
F30 JUMPERS
J3
FPA 32
J2 - 2
J4
FPA 33
J2 - 3
J5
FPA 41
J2 8,9,10
J6
FPA 36
FPA 39
J7
FPA 30
FPA 40
J2 - 1
F-Sync
FPA - 25
Line Clock
FPA - 26
Reset Clock
FPA - 28
L-Sync
FPA - 43
Pixel Clock
FPA - 42
Read Clock
FPA - 27
Digital PWR
FPA - 34
connector locking pin
J1 IDE 10P
9
8
4
3
2
7
1
10
Bias and Clocks Internal cable # 2
S1-coax
.005 Constantan
Heatsinks
18 pin
A
L
D
R
E
F
B
N
C
P
K
M
G
H
Bias and Clocks External cable # 2
RG174-coax
20 AWG copper
25S
25P
1
9
4
12
5
13
2
10
3
11
6
15
7
8
Clock Driver Board
37S
4
Fsync
25
Fsync shield
2
Line Clock
23
Line Clock shield
1
Reset
22
Reset shield
3
Lsync
24
Lsync shield
5
Pixel Clock
26
Pixel Clock shield
6
Read
22
Read shield
32
Vss (digital
29
Case ground

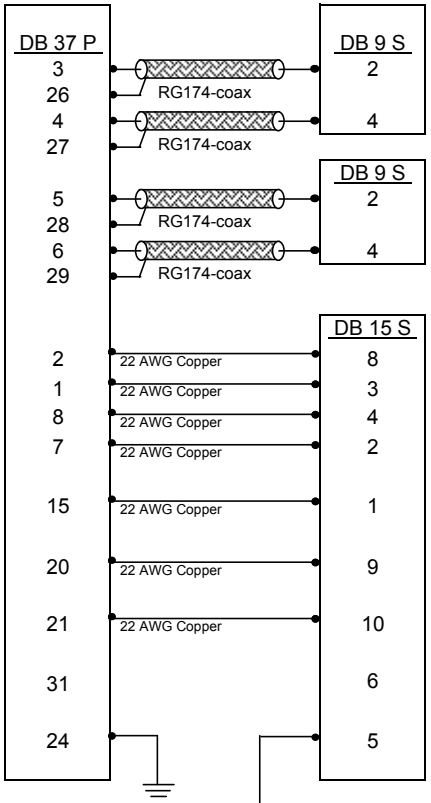
Outputs internal cable # 1



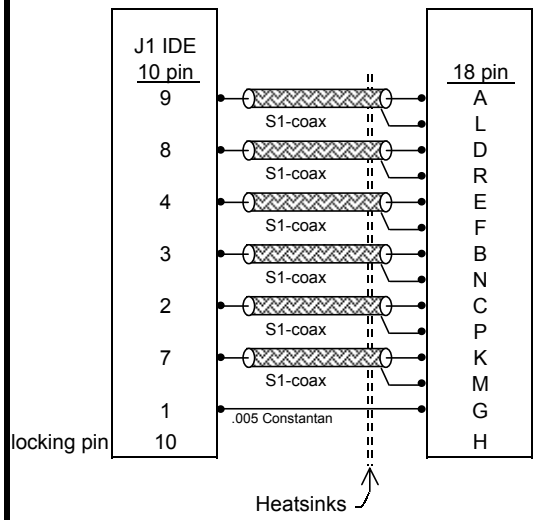
Outputs external cable # 1



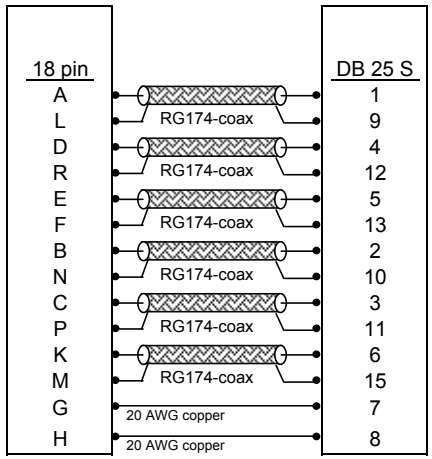
Camera electronics

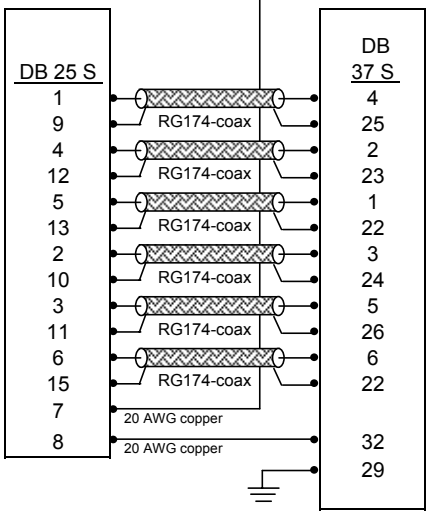


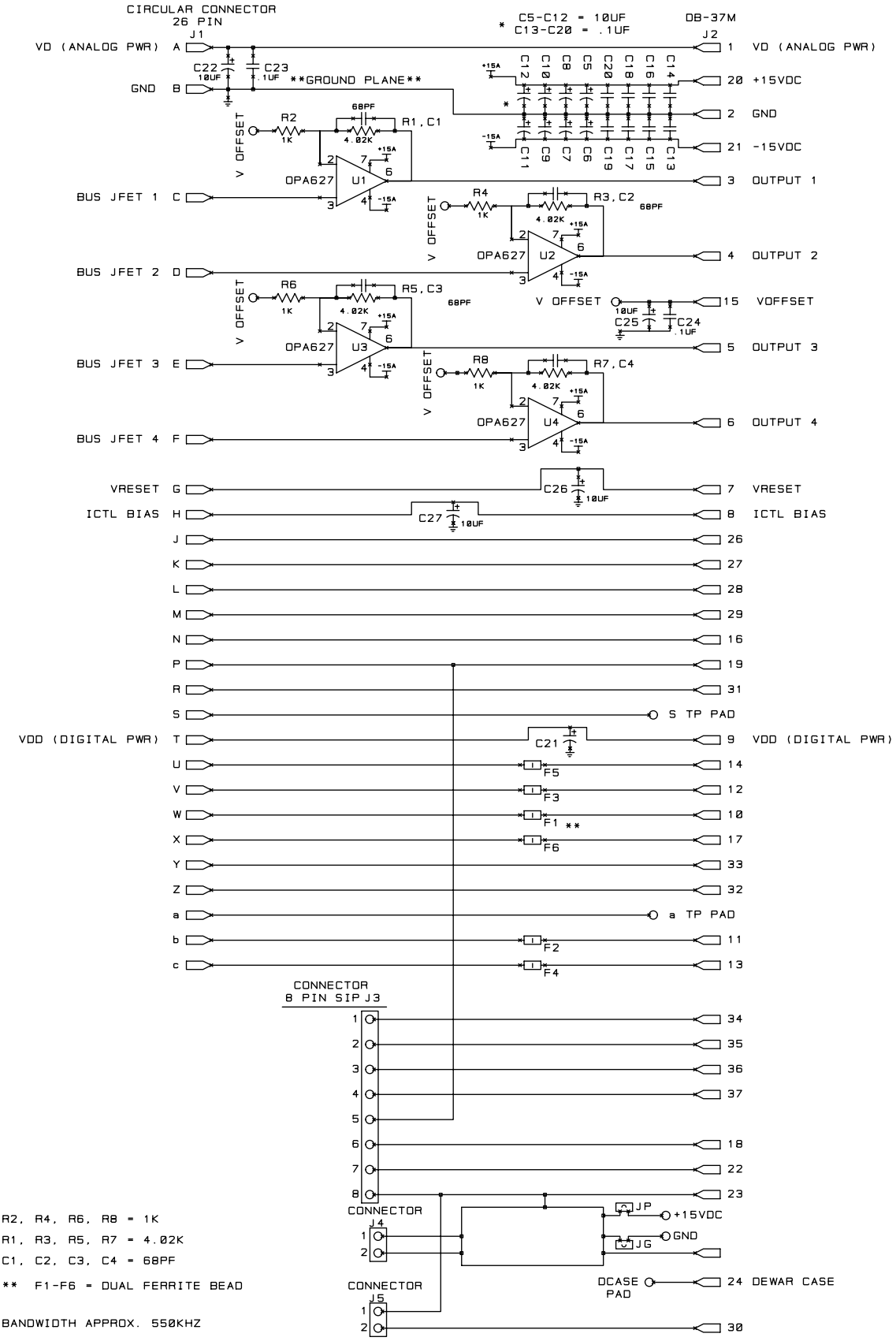
Bias and Clocks Internal cable # 2



Bias and Clocks External cable # 2







IREM1-B DEWAR INTERFACE PREAMP BOARD

INFRARED LABORTORIES, INC. 1808 E. 17TH. STREET TUCSON, AZ. 85719 USA	
PROJECT:	PREAMP
DESC.:	PREAMP AUX BOARD PREAMP CIRCUIT BOARD
PAUL ARBO	REV.: C
PAGE: 1 OF 1	DATE: 9-30-97

IREM1 - B, Preamp